7 Series FPGAs Packaging and Pinout

Product Specification

UG475 (v1.9) February 14, 2013

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/11	1.0	Initial Xilinx release.
04/06/11	1.1	Removed the SBG324 package from the entire document. Added three Kintex-7 devices: XC7K355T, XC7K420T, and XC7K480T. Updated disclaimer and copyright on page 2. Updated package size of FF1156 in Table 1-1. Updated DXP_0, DXN_0 in Table 1-13. The Table 2-2 single ASCII device files have been updated for both the XC7K70T and XC7K160T. All ASCII TXT files and the overall ZIP file have been updated on the web. Updated the XC7K70TFBG676 figures: Figure 3-37, Figure 3-38, Figure 3-39, and Figure 3-40. Added information to Chapter 4, Mechanical Drawings, Chapter 5, Thermal Specifications, and Chapter 6, Package Marking.

Date	Version	Revision
06/14/11	1.2	Added Virtex-7 device information including updating Table 1-1, adding Table 1-3, Table 1-10, Table 2-3, and Table 3-3. In Table 1-13, updated Note 3, the Configuration Pins section, and the Analog to Digital Converter (XADC) Pins section. Updated Figure 3-35, Figure 3-36, Figure 3-39, Figure 3-40, Figure 3-43, Figure 3-44, Figure 3-47, Figure 3-48, Figure 3-51, Figure 3-52, Figure 3-55, and Figure 3-56. Added Figure 3-56 through Figure 3-120. Added Figure 4-24 the mechanical drawing for the Kintex-7 devices FFG1156 package. Also added some Virtex-7 device mechanical drawings in Figure 4-24 through Figure 4-28. Added thermal resistance data to Table 5-1.
10/03/11	1.3	Added Artix-7 device information including updating Table 1-1, adding Table 1-3, Table 1-8, Table 2-1, and Table 3-1. Clarified the interposer in Figure-12 and Figure 1-11. Revised horizontal center for the XC7VX415T in Figure 1-13. Updated the DXP_0, DXN_0 description and notes in Table 1-13. Added devices to the Die Level Bank Numbering Overview section. Clarified the I/O banks summary section. Added Artix-7 device diagrams in the CSG324 package. Added XC7V585T device diagrams Figure 3-69 through Figure 3-76. Moved AD4P/N, AD12P/N, and AD5P/N pins from [IO_L2P_T0_35:IO_L4N_T0_35] to [IO_L1P_T0_35:IO_L3N_T0_35] in Figure 3-77, Figure 3-81, Figure 3-101, Figure 3-105, Figure 3-109, Figure 3-113, and Figure 3-117. Fixed the labeling for EMCCLK in Figure 3-61, Figure 3-69, Figure 3-77, Figure 3-81, Figure 3-101, Figure 3-105, Figure 3-109, Figure 3-113, and Figure 3-117. Updated the mechanical drawings for Figure 4-26 and Figure 4-28. Updated thermal resistance data in Table 5-1. Updated Chapter 6, Package Marking.
10/17/11	1.4	Revised the FBG484 Package section describing XC7K160T Banks. Added the mechanical drawings: Figure 4-26 and Figure 4-29. Updated Figure 4-28 to include the FF(G)1928 package. Added thermal resistance data to Table 5-1.
02/03/12	1.5	Updated Table 1-3 and Table 1-5 and added Table 1-6. Updated Table 1-7 and Table 1-9 and added Table 1-10. Revised Note 2 in Table 1-13. Removed Figures 1-1 and 1-2 along with references to the XC7A8, XC7A15, XC7A30T, and XC7A50T. Added Figure 1-2 and Figure 1-3. Clarified Figure 1-6 though Figure 1-9, Figure 1-11, Figure 1-15, and Figure 1-18. Updated Table 2-3 and added Table 2-4. Added devices to Table 3-1 and revised Table 3-2 (XC7K420T and XC7K480T). Updated Table 3-3 and added Table 3-4 and Table 3-5. Revised specifications in: • Figure 4-11: FB/FBG484 Flip-Chip Lidless BGA (Kintex-7 FPGAs) (1.0 mm Pitch) • Figure 4-14: FB/FBG676 Flip-Chip Lidless BGA (Kintex-7 FPGAs) (1.0 mm Pitch). • Figure 4-19: FB/FBG900 Flip-Chip Lidless BGA (Kintex-7 FPGAs) (1.0 mm Pitch) and combined with Figure 4-6. • Figure 4-25: FF/FFG1157 and FF/FFG1158 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch). Added thermal resistance data to Table 5-1 and added Soldering Guidelines section. Added Appendix B.

Date	Version	Revision

05/24/12	1.6	Removed the FFG1933 and FLG1933 packages throughout. Added the FLG1926 package where appropriate.
		Updated the Introduction in Chapter 1. Updated XC7K420T in Table 1-10. Added Note 6 to Table 1-13. Updated the description and figure in the XC7K420T Banks and XC7VX550T Banks sections.
		Updated Figure 3-22, Figure 3-26, Figure 3-30, and Figure 3-34. Added Figure 3-145 through Figure 3-148.
		Added Figure 4-6: FB/FBG676 Flip-Chip Lidless BGA Package Specifications for Artix-7 FPGAs. Revised specifications and added capacitor location figures for:
		• Figure 4-14: FB/FBG676 Flip-Chip Lidless BGA Package Specifications for Kintex-7 FPGAs
		  • Figure 4-17: XC7K325T FB/FBG676 Die Dimensions with Capacitor Locations
		  • Figure 4-18: XC7K410T FB/FBG676 Die Dimensions with Capacitor Locations
		• Figure 4-19: FB/FBG900 Flip-Chip Lidless BGA Package Specifications for Kintex-7 FPGAs
		  • Figure 4-20: XC7K325T FB/FBG900 Die Dimensions with Capacitor Locations
		  • Figure 4-21: XC7K410T FB/FBG900 Die Dimensions with Capacitor Locations
		• Figure 4-24: FF/FFG1156 Flip-Chip BGA Package Specification for Kintex-7 FPGAs
		• Figure 4-25: FF/FFG1157 and FF/FFG1158 Flip-Chip BGA Package Specification for Virtex-7 FPGAs
		Added Thermal Management Strategy, Some Thermal Management Options, and updated Soldering Guidelines in Chapter 5.
		Updated Table A-1.

07/20/12	1.7	In Table 1-13, updated the Other Pins section. Added the XC7VH290T, XC7VH580T, and XC7VH870T and associated HCG packages to all appropriate chapters, tables, and figures. Added the SBG484 package for the XC7A200T devices to all appropriate chapters, tables, and figures. Updated the XC7VX1140T-FLG1926 headings in Table 2-4, Figure 3-145 through Figure 3-148, and Figure 4-29. Updated GTP Quad numbers in Figure 1-1, Figure 3-10, and Figure 3-14. Also added numbers to Figure 3-13 and Figure 3-16. Updated the XC7V585T-FFG1761 figures: Figure 3-73 and Figure 3-76. Added new mechanical drawings for the Artix-7 FPGAs in Chapter 4 along with Figure 4-16, Figure 4-30, and Figure 4-31, and updated Figure 4-23. In Table 5-1, updated data throughout and added XC7VX1140T (FL1926) and XC7VH580T data. Added Figure 6-3: Artix-7 Device Package Marking.
10/15/12	1.8	Removed the following devices: XC7A350T, XC7V1500T, XC7VH290T. Added Figure 4-15 and updated drawing in Figure 4-16. Added Note 5 to Figure 4-25. Updated A2 dimension in Figure 4-28. Updated aaa dimension in Figure 4-27 and Figure 4-29. Updated the JEDEC Moisture Sensitivity Level (MSL) for the Flip-Chip packages on page 270.

Date	Version	Revision
02/14/13	1.9	Clarified pins in Figure 3-25. Updated Figure 4-10 and Figure 4-11 and added Figure 4-12 and Figure 4-13. Revised Figure 4-23 and Figure 4-25. In Table 5-1, updated data for Artix-7 FPGAs, XC7K160T FF/FFG676, Virtex-7 T FPGAs and XC7VX1140T. Updated Appendix B.

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Chapter 2: 7 Series FPGAs Package Files

Chapter 3: Device Diagrams

Chapter 4: Mechanical Drawings

Chapter 5: Thermal Specifications

About This Guide

Xilinx® 7 series FPGAs include three unified FPGA families that are all designed for lowest power to enable a common design to scale across families for optimal power, performance, and cost. The Artix™-7 family is optimized for lowest cost and absolute power for the highest volume applications. The Virtex®-7 family is optimized for highest system performance and capacity. The Kintex™-7 family is an innovative class of FPGAs optimized for the best price-performance. This guide serves as a technical reference describing the 7 series packaging and pinout specifications.

This 7 series packaging and pinout specification, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at www.xilinx.com/7.

Guide Contents

This manual contains the following chapters:

- Chapter 1, Packaging Overview
- Chapter 2, 7 Series FPGAs Package Files
- Chapter 3, Device Diagrams
- Chapter 4, Mechanical Drawings
- Chapter 5, Thermal Specifications
- Chapter 6, Package Marking
- Appendix A, Recommended PCB Design Rules for BGA Packages

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

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Chapter 1

Packaging Overview

Summary

This chapter covers the following topics:

- Introduction
- Device/Package Combinations and Maximum I/Os
- Pin Definitions
- Pin Compatibility Between Packages
- Die Level Bank Numbering Overview

Introduction

This section describes the pinouts for the 7 series FPGAs in various fine pitch and flip-chip 1.0 mm pitch BGA packages and 0.8 mm pitch chip scale packages.

Artix™-7 and Kintex™-7 devices are offered in low-cost, space-saving packages that are optimally designed for the maximum number of user I/Os.

Virtex®-7 T and Virtex-7 XT devices are offered exclusively in high performance flip-chip BGA packages that are optimally designed for improved signal integrity and jitter. The Virtex-7 HT devices are offered in ceramic flip-chip, fine-pitch BGA packages.

Package inductance is minimized as a result of optimal placement and even distribution as well as an increased number of Power and GND pins.

All packages are available as Pb-free (additional G in package name) with selected packages including a Pb-only option.

All of the 7 series devices supported in a particular package are pinout compatible. Pins that are available in a device but are not available in a smaller device with a compatible package are listed as “No Connects”.

Each device is split into I/O banks to allow for flexibility in the choice of I/O standards (see UG471, *7 Series FPGAs SelectIO Resources User Guide*). Table 1-13 provides definitions for all pin types.

Device/Package Combinations and Maximum I/Os

Table 1-1 shows the maximum number of user I/Os possible in the 7 series FPGAs BGA packages. Some devices are available in both Pb and Pb-free (additional G) packages as standard ordering options.

Table 1-1: **7 Series FPGAs Package Specifications**

Packages[1]	Description	Package Specifications			
		Package Type	Pitch (mm)	Size (mm)	Maximum I/Os[2]
CSG324	Wire-bond chip-scale	BGA	0.8	15 x 15	210
FTG256	Wire-bond fine-pitch	BGA	1.0	17 x 17	170
FGG484		BGA	1.0	23 x 23	285
FGG676		BGA	1.0	27 x 27	300
SBG484	Flip-chip lidless	BGA	0.8	19 x 19	285
FB484/FBG484		BGA	1.0	23 x 23	285
FB676/FBG676		BGA	1.0	27 x 27	400
FB900/FBG900		BGA	1.0	31 x 31	500
FF676/FFG676	Flip-chip fine-pitch	BGA	1.0	27 x 27	400
FF900/FFG900		BGA	1.0	31 x 31	500
FF901/FFG901		BGA	1.0	31 x 31	380
FF1156/FFG1156		BGA	1.0	35 x 35	600
FF1157/FFG1157		BGA	1.0	35 x 35	600
FF1158/FFG1158		BGA	1.0	35 x 35	350
FF1761/FFG1761		BGA	1.0	42.5 x 42.5	850
FF1926/FFG1926		BGA	1.0	45 x 45	720
FF1927/FFG1927		BGA	1.0	45 x 45	600
FF1928/FFG1928		BGA	1.0	45 x 45	480
FF1930/FFG1930		BGA	1.0	45 x 45	1000
FL1925/FLG1925		BGA	1.0	45 x 45	1200
FL1926/FLG1926		BGA	1.0	45 x 45	720
FL1928/FLG1928		BGA	1.0	45 x 45	480
FL1930/FLG1930		BGA	1.0	45 x 45	1100
FH1761/FHG1761		BGA	1.0	45 x 45	850
HCG1931	Ceramic Flip-chip fine-pitch	BGA	1.0	45 x 45	650
HCG1932		BGA	1.0	45 x 45	300

Notes:

1. Leaded package options (FFxxx/FBxxx) are available for the Kintex-7 XC7K160T, XC7K325T, XC7K355T, XC7K410T, XC7K420T, and XC7K480Tdevices.
2. The maximum I/O numbers do not include pins in the configuration Bank 0 (Table 1-2) or the GTX serial transceivers.

Table 1-2 lists the 21 dedicated I/O pins.

Table 1-2: **7 Series FPGAs I/O Pins in the Dedicated Configuration Bank (Bank0)**

DXP_0	VCCBATT_0	INIT_B_0	M0_0	TDO_0	TDI_0	GNDADC_0
DXN_0	DONE_0	VN_0	M1_0	TCK_0	VREFN_0	VCCADC_0
PROGRAM_B_0	CCLK_0	VP_0	M2_0	TMS_0	VREFP_0	CFGBVS_0

Serial Transceiver Channels by Device/Package

Table 1-3 lists the quantity of GTP serial transceiver channels for the Artix-7 FPGAs.

Table 1-3: **Serial Transceiver Channels (GTPs) by Device/Package (Artix-7 FPGAs)**

Device	GTP Channels by Package							
	CSG324	FTG256	SBG484	FGG484	FGG676	FBG484	FBG676	FFG1156
XC7A100T	0	0	–	4	8	–	–	–
XC7A200T	–	–	4	–	–	4	8	16

Table 1-4 lists the quantity of GTX serial transceiver channels for the Kintex-7 FPGAs.

Table 1-4: **Serial Transceiver Channels (GTXs) by Device/Package (Kintex-7 FPGAs)**

Device	GTX Channels by Package						
	FBG484	FBG676	FBG900	FFG676	FFG900	FFG901	FFG1156
XC7K70T	4	8	–	–	–	–	–
XC7K160T	4	8	–	8	–	–	–
XC7K325T	–	8	16	8	16	–	–
XC7K355T	–	–	–	–	–	24	–
XC7K410T	–	8	16	8	16	–	–
XC7K420T	–	–	–	–	–	28	32
XC7K480T	–	–	–	–	–	28	32

Table 1-5 lists the quantity of GTX serial transceiver channels for the Virtex-7 T FPGAs.

Table 1-5: **Serial Transceiver Channels (GTX) by Device/Package (Virtex-7 T FPGAs)**

Device	FFG1157	FFG1761	FLG1925	FHG1761
XC7V585T	20	36	–	–
XC7V2000T	–	–	16	36

Table 1-6 lists the quantity of GTX and GTH serial transceiver channels for the Virtex-7 XT FPGAs. In all devices, a serial transceiver channel is one set of MGTRXP, MGTRXN, MGTTXP, and MGTTXN pins.

Table 1-6: **Serial Transceiver Channels (GTX/GTH) by Device/Package (Virtex-7 XT FPGAs)**

Device	FFG 1157		FFG 1158		FFG 1761		FFG 1926		FFG 1927		FFG 1928		FFG 1930		FLG 1926		FLG 1928		FLG 1930	
	GTX	GTH	GTX	GTH	GTX	GTH	GTX	GTH	GTX	GTH	GTX	GTH	GTX	GTH	GTX	GTH	GTX	GTH	GTX	GTH
XC7VX330T	0	20	–		0	28	–		–		–		–		–		–		–	
XC7VX415T	0	20	0	48	–		–		0	48	–		–		–		–		–	
XC7VX485T	20	0	48	0	28	0	–		56	0	–		24	0	–		–		–	
XC7VX550T	–		0	48	–		–		0	80	–		–		–		–		–	
XC7VX690T	0	20	0	48	0	36	0	64	0	80	–		0	24	–		–		–	
XC7VX980T	–		–		–		0	64	–		0	72	0	24	–		–		–	
XC7VX1140T	–		–		–		–		–		–		–		0	64	0	96	0	24

Table 1-7 lists the quantity of GTH and GTZ serial transceiver channels for the Virtex-7 HT FPGAs.

Table 1-7: **Serial Transceiver Channels (GTH/GTZ) by Device/Package (Virtex-7 HT FPGAs)**

Device	HCG1155		HCG1931		HCG1932	
	GTH	GTZ	GTH	GTZ	GTH	GTZ
XC7VH580T	24	8	48	8	48	8
XC7VH870T	–		48	8	72	16

Table 1-8 shows the number of available I/Os and the number of differential I/Os for each Artix-7 device/package combination.

Table 1-8: **Available I/O Pin/Device/Package Combinations for Artix-7 FPGAs**

Artix-7 Devices	User I/O Pins	Artix-7 FPGA Packages: HR I/O Banks Only							
		CSG324	FTG256	SBG484	FGG484	FGG676	FBG484	FBG676	FFG1156
XC7A100T	User I/O	210	170	–	285	300	–	–	–
	Differential	202	163	–	274	288	–	–	–
XC7A200T	User I/O	–	–	285	–	–	285	400	500
	Differential	–	–	274	–	–	274	384	480

Table 1-9 shows the number of available I/Os and the number of differential I/Os for each Kintex-7 device/package combination.

Table 1-9: **Available I/O Pin/Device/Package Combinations for Kintex-7 FPGAs**

Kintex-7 Devices	User I/O Pins	Kintex-7 FPGA Packages: HR and HP I/O Banks													
		FBG484		FBG676		FBG900		FFG676		FFG900		FFG901		FFG1156	
		HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR
XC7K70T	User I/O	100	185	100	200	–	–	–	–	–	–	–	–	–	–
	Differential	96	179	96	192	–	–	–	–	–	–	–	–	–	–
XC7K160T	User I/O	100	185	150	250	–	–	150	250	–	–	–	–	–	–
	Differential	96	179	144	240	–	–	144	240	–	–	–	–	–	–
XC7K325T	User I/O	–	–	150	250	150	350	150	250	150	350	–	–	–	–
	Differential	–	–	144	240	144	336	144	240	144	336	–	–	–	–
XC7K355T	User I/O	–	–	–	–	–	–	–	–	–	–	0	300	–	–
	Differential	–	–	–	–	–	–	–	–	–	–	0	288	–	–
XC7K410T	User I/O	–	–	150	250	150	350	150	250	150	350	–	–	–	–
	Differential	–	–	144	240	144	336	144	240	144	336	–	–	–	–
XC7K420T	User I/O	–	–	–	–	–	–	–	–	–	–	0	380	0	400
	Differential	–	–	–	–	–	–	–	–	–	–	0	366	0	384
XC7K480T	User I/O	–	–	–	–	–	–	–	–	–	–	0	380	0	400
	Differential	–	–	–	–	–	–	–	–	–	–	0	366	0	384

Table 1-10, Table 1-11, and Table 1-12 show the number of available I/Os and the number of differential I/Os for each Virtex-7 device/package combination. When applicable, it also lists the number of user I/Os in the 3.3V-capable high-range (HR) banks and the number of 1.8V-capable high-performance (HP) banks.

Table 1-10: **Available I/O Pin/Device/Package Combinations for Virtex-7 T FPGAs**

Virtex-7 T Devices	User I/O Pins	Virtex-7 T FPGA Packages: HR and HP I/O Banks							
		FFG		FFG		FLG		FHG	
		1157		1761		1925		1761	
		HP	HR	HP	HR	HP	HR	HP	HR
XC7V585T	User I/O	600	0	750	100	–		–	
	Differential	576	0	720	96	–		–	
XC7V2000T	User I/O	–		–		1200	0	850	0
	Differential	–		–		1152	0	816	0

Table 1-11: **Available I/O Pin/Device/Package Combinations for Virtex-7 XT FPGAs**

Virtex-7 XT Devices	User I/O Pins	Virtex-7 XT FPGA Packages: HR and HP I/O Banks																			
		FFG		FFG		FFG		FFG		FFG		FFG		FFG		FLG		FLG		FLG	
		1157		1158		1761		1926		1927		1928		1930		1926		1928		1930	
		HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR
XC7VX330T	User I/O	600	0	–		650	50	–		–		–		–		–		–		–	
	Differential	576	0	–		624	48	–		–		–		–		–		–		–	
XC7VX415T	User I/O	600	0	350	0	–		–		600	0	–		–		–		–		–	
	Differential	576	0	336	0	–		–		576	0	–		–		–		–		–	
XC7VX485T	User I/O	600	0	350	0	700	0	–		600	0	–		700	0	–		–		–	
	Differential	576	0	336	0	672	0	–		576	0	–		672	0	–		–		–	
XC7VX550T	User I/O	–		350	0	–		–		600	0	–		–		–		–		–	
	Differential	–		336	0	–		–		576	0	–		–		–		–		–	
XC7VX690T	User I/O	600	0	350	0	850	0	720	0	600	0	–		1000	0	–		–		–	
	Differential	576	0	336	0	816	0	690	0	576	0	–		960	0	–		–		–	
XC7VX980T	User I/O	–		–		–		720	0	–		480	0	900	0	–		–		–	
	Differential	–		–		–		690	0	–		460	0	864	0	–		–		–	
XC7VX1140T	User I/O	–		–		–		–		–		–		–		720	0	480	0	1100	0
	Differential	–		–		–		–		–		–		–		690	0	460	0	1056	0

Table 1-12: **Available I/O Pin/Device/Package Combinations for Virtex-7 HT FPGAs**

Virtex-7 HT Devices	User I/O Pins	Virtex-7 HT FPGA Packages: HP I/O Banks Only		
		HCG1155	HCG1931	HCG1932
XC7VH580T	User I/O	400	600	300
	Differential	384	576	288
XC7VH870T	User I/O	–	650	300
	Differential	–	624	288

Pin Definitions

Table 1-13 lists the pin definitions used in 7 series FPGAs packages.

Note: There are dedicated general purpose user I/O pins listed separately in Table 1-13. There are also multi-function pins where the pin names start with either IO_LXXY_ZZZ_# or IO_XX_ZZZ_#, where ZZZ represents one or more functions in addition to being general purpose user I/O. If not used for their special function, these pins can be user I/O.

Table 1-13: **7 Series FPGAs Pin Definitions**

Pin Name	Type	Direction	Description
User I/O Pins			
IO_LXXY_# IO_XX_#	Dedicated	Input/ Output	Most user I/O pins are capable of differential signaling and can be implemented as pairs. The top and bottom I/O pins are always single ended. Each user I/O is labeled IO_LXXY_#, where: • IO indicates a user I/O pin. • L indicates a differential pair, with XX a unique pair in the bank and Y = [P | N] for the positive/negative sides of the differential pair. • # indicates a bank number.
Configuration Pins			
For more information, see the *Configuration Pin Definitions* table in UG470, *7 Series FPGAs Configuration User Guide*.			
CCLK_0	Dedicated(1)	Input/ Output	Configuration clock. Output in Master mode or input in Slave mode.
DONE_0	Dedicated(1)	Bidirectional	Active High, DONE indicates successful completion of configuration.
INIT_B_0	Dedicated(1)	Bidirectional (open-drain)	Active Low, indicates initialization of configuration memory.
M0_0, M1_0, or M2_0	Dedicated(1)	Input	Configuration mode selection.
PROGRAM_B_0	Dedicated(1)	Input	Active Low, asynchronous reset to configuration logic.
TCK_0	Dedicated(1)	Input	JTAG clock.
TDI_0	Dedicated(1)	Input	JTAG data input.
TDO_0	Dedicated(1)	Output	JTAG data output.
TMS_0	Dedicated(1)	Input	JTAG mode select.
CFGBVS_0	Dedicated(1)	Input	This pin selects the preconfiguration I/O standard type for the dedicated and multi-function configuration banks 0, 14, and 15. If the V_{CCO} for banks 0, 14, or 15 is 2.5V or 3.3V, then this pin must be connect to V_{CCO_0}. If the V_{CCO} for banks 0, 14, and 15 are less than or equal to 1.8V, then this pin should be connected to GND. ***Note:*** To avoid device damage, this pin must be connected correctly. See the *Configuration Bank Voltage Select* section in UG470: *7 Series FPGAs Configuration User Guide* for more information.
D00 through D31	Multi-function	Bidirectional	Configuration data pins.

Table 1-13: **7 Series FPGAs Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
ADV_B	Multi-function	Output	BPI Flash address valid output.
A00 through A28	Multi-function	Output	Address A00–A28 BPI address output.
RS0 or RS1	Multi-function	Output	RS0 and RS1 revision select output.
FCS_B	Multi-function	Output	BPI and SPI flash chip select.
FOE_B	Multi-function	Output	BPI flash output enable.
MOSI	Multi-function	Output	SPI flash command output. Also known as the SPI bus master output, slave input signal.
FWE_B	Multi-function	Output	BPI flash write enable.
DOUT	Multi-function	Output	Data output for serial daisy-chain configuration.
CSO_B	Multi-function	Output	Active Low chip-select output for parallel daisy-chain.
CSI_B	Multi-function	Input	SelectMAP active Low chip-select input.
PUDC_B	Multi-function	Input	Active Low input enables internal pull-ups during configuration on all SelectIO pins: 0 = Weak preconfiguration I/O pull-up resistors enabled 1 = Weak preconfiguration I/O pull-up resistors disabled
RDWR_B	Multi-function	Input	SelectMAP data bus direction control signal for reading or writing configuration data.
EMCCLK	Multi-function	Input	External master configuration clock.
Power/Ground Pins			
GND	Dedicated	N/A	Ground.
VCCAUX	Dedicated	N/A	1.8V power-supply pins for auxiliary circuits.
VCCAUX_IO_G#(2)	Dedicated	N/A	1.8V/2.0V power-supply pins for auxiliary I/O circuits.
VCCINT	Dedicated	N/A	0.9V/1.0V power-supply pins for the internal core logic.
VCCO_#(3)	Dedicated	N/A	Power-supply pins for the output drivers (per bank).
VCCBRAM	Dedicated	N/A	1.0V power-supply pins for the FPGA logic block RAM.
VCCBATT_0	Dedicated	N/A	Decryptor key memory backup supply; this pin should be tied to the appropriate V_{CC} or GND when not used(4).
VREF	Multi-function	N/A	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Analog to Digital Converter (XADC) Pins			
For more information, see the *XADC Package Pins* table in UG480, *7 Series FPGAs XADC User Guide*.			
VCCADC_0(5)	Dedicated	N/A	XADC analog positive supply voltage.
GNDADC_0(5)	Dedicated	N/A	XADC analog ground reference.
VP_0(5)	Dedicated	Input	XADC dedicated differential analog input (positive side).
VN_0(5)	Dedicated	Input	XADC dedicated differential analog input (negative side).

Table 1-13: **7 Series FPGAs Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
VREFP_0[5]	Dedicated	N/A	1.25V reference input.
VREFN_ 0[5]	Dedicated	N/A	1.25V reference GND reference.
AD0P through AD15P AD0N through AD15N	Multi-function	Input	XADC (analog-to-digital converter) differential auxiliary analog inputs 0–15. Auxiliary channels 6, 7, 13, 14, and 15 are not supported on Kintex-7 devices.
Multi-gigabit Serial Transceiver Pins (GTXE2 and GTHE2)			
For more information on the GTXE2 and GTHE2 pins see the *Pin Description and Design Guidelines* section in UG476, *7 Series FPGAs GTX/GTH Transceivers User Guide*.			
MGTXRXP[0:3]	Dedicated	Input	Positive differential receive port GTX Quad.
MGTXRXN[0:3]	Dedicated	Input	Negative differential receive port GTX Quad.
MGTXTXP[0:3]	Dedicated	Output	Positive differential transmit port GTX Quad.
MGTXTXN[0:3]	Dedicated	Output	Negative differential transmit port GTX Quad.
MGTHRXP[0:3]	Dedicated	Input	Positive differential receive port GTH Quad.
MGTHRXN[0:3]	Dedicated	Input	Negative differential receive port GTH Quad.
MGTHTXP[0:3]	Dedicated	Output	Positive differential transmit port GTH Quad.
MGTHTXN[0:3]	Dedicated	Output	Negative differential transmit port GTH Quad.
MGTAVCC_G#[6]	Dedicated	Input	1.0V analog power-supply pin for the receiver and transmitter internal circuits.
MGTAVTT_G#[6]	Dedicated	Input	1.2V analog power-supply pin for the transmit driver.
MGTVCCAUX_G#[6]	Dedicated	Input	1.8V auxiliary analog Quad PLL (QPLL) voltage supply for the transceivers.
MGTREFCLK0/1P	Dedicated	Input	Positive differential reference clock for the transceivers.
MGTREFCLK0/1N	Dedicated	Input	Negative differential reference clock for the transceivers.
MGTAVTTRCAL	Dedicated	N/A	Precision reference resistor pin for internal calibration termination. Not used for Artix-7 devices.
MGTRREF	Dedicated	Input	Precision reference resistor pin for internal calibration termination.
GTZE2 Octal Transceiver Pins			
For more information on the GTZ transceivers see UG478, *7 Series FPGAs GTZ Transceivers User Guide*.			
MGTZRXP	Dedicated	Input	Positive differential receive port GTZ Octal.
MGTZRXN	Dedicated	Input	Negative differential receive port GTZ Octal.
MGTZTXP	Dedicated	Output	Positive differential transmit port GTZ Octal.
MGTZTXN	Dedicated	Output	Negative differential transmit port GTZ Octal.
MGTZAGND	Dedicated	Input	Analog ground connection.

Table 1-13: **7 Series FPGAs Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
MGTZAVCC	Dedicated	Input	1.0V analog power-supply pin for the receiver and transmitter internal circuits.
MGTZVCCH	Dedicated	Input	1.8V power-supply pin for the I/O circuits.
MGTZVCCL	Dedicated	Input	1.0V digital power-supply pin for the receiver and transmitter internal circuits.
MGTZ_SENSE_AGND	Dedicated	Output	Reference pin for MGTZ_SENSE_AVCC.
MGTZ_SENSE_AVCC	Dedicated	Output	Sense voltage pin for MGTZAVCC.
MGTZ_SENSE_VCCH	Dedicated	Output	Sense pin for die MGTZVCCH voltage.
MGTZ_SENSE_VCCL	Dedicated	Output	Sense pin for die MGTZVCCL voltage.
MGTZ_SENSE_VCC	Dedicated	Output	Sense pin for die V_{CCINT} voltage.
MGTZREFCLK0/1P	Dedicated	Input	Positive differential reference clock for the transceivers.
MGTZREFCLK0/1N	Dedicated	Input	Negative differential reference clock for the transceivers.
MGTZ_THERM_IN	Dedicated	Input	Temperature-sensing diode pin (anode).
MGTZ_THERM_OUT	Dedicated	Output	Temperature-sensing diode pin (cathode).
MGTZ_OBS_CLK_P	Dedicated	Output	Reserved. No Connection; leave floating.
MGTZ_OBS_CLK_N	Dedicated	Output	Reserved. No Connection; leave floating.
Other Pins			
MRCC	Multi-function	Input	These are the clock capable I/Os driving BUFRs, BUFIOs, BUFGs, and MMCMs/PLLs. In addition, these pins can drive the BUFMR for multi-region BUFIO and BUFR support. These pins become regular user I/Os when not needed as a clock. When connecting a single-ended clock to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. The MRCC (multi-region) pins, when used as single region resource, can drive four BUFIOs and four BUFR in a single bank.
SRCC	Multi-function	Input	These are the clock capable I/Os driving BUFRs, BUFIOs, and MMCMs/PLLs. These pins become regular user I/Os when not needed for clocks. When connecting a single-ended clock to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. The SRCC (single region) pins can drive four BUFIOs and four BUFRs in a single bank.
VRN[(7)]	Multi-function	N/A	This pin is for the DCI voltage reference resistor of N transistor (per bank, to be pulled High with reference resistor).
VRP[(7)]	Multi-function	N/A	This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with reference resistor).

Table 1-13: **7 Series FPGAs Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
DXP_0, DXN_0	Dedicated	Input	Temperature-sensing diode pins (Anode: DXP; Cathode: DXN). The thermal diode is accessed by using the DXP and DXN pins in bank 0. When not used, tie to GND. To use the thermal diode an appropriate external thermal monitoring IC must be added. Consult the external thermal monitoring IC data sheet for usage guidelines. The recommended temperature monitoring solution for 7 series FPGAs uses the temperature sensor in the XADC block.
T0, T1, T2, or T3	Multi-function	Input	This pin belongs to the memory byte group 0-3.
T0_DQS, T1_DQS, T2_DQS, or T3_DQS	Multi-function	Input	The DDR DQS strobe pin that belongs to the memory byte group T0–T3.

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CCO_0}.
2. For devices that do not include VCCAUX_IO_G# pins, auxiliary I/O circuits are powered by VCCAUX pins. As indicated in Chapter 2, 7 Series FPGAs Package Files, some packages include VCCAUX_IO_G# pins but also have auxiliary I/O circuits powered by VCCAUX pins. In this case, the VCCAUX_IO_G# pins exist for migration purposes only and will not connect to any internal circuitry.
3. V_{CCO} pins in unbonded banks must be connected to the V_{CCO} for that bank for package migration. Do NOT connect unbonded V_{CCO} pins to different supplies. Without a package migration requirement, V_{CCO} pins in unbonded banks can be tied to a common supply (V_{CCO} or ground).
4. Refer to the data sheet for V_{CCBATT_0} specifications.
5. See UG480, *7 Series FPGAs XADC User Guide* for the default connections required to support on-chip monitoring.
6. In packages with only one MGT power group, the MGTAVCC_G#, MGTAVTT_G#, and MGTVCCAUX_G# pins are labeled without the _G#. These pins also appear without a number in the power and GND placement diagrams in Chapter 3, Device Diagrams.
7. The DCI guidelines in the 7 series FPGAs are different from previous Virtex device DCI guidelines. See the DCI sections in UG471: *7 Series FPGAs SelectIO Resources User Guide* for more information on the VRN/VRP pins.

Pin Compatibility Between Packages

7 series FPGA devices are pin compatible only with other 7 series FPGA devices of the same family (Artix-7, Kintex-7, and Virtex-7) in the same package. In addition, FB/FBG, FF/FFG, FH/FHG, and FL/FLG packages of the same pin-count designator are pin compatible.

Note: Pin compatible packages can have substantially different decoupling capacitor recommendations.

Some FB/FBG packages include V_{CCAUX_IO} pins that are not utilized by the I/O. These pins are placeholders to ensure pin compatibility with FF/FFG packages. In the FF/FFG packages, when the high-performance option is chosen for the HP I/O banks, the V_{CCAUX_IO} pins must be connected to a separate power supply from V_{CCAUX}. Therefore, to allow for migration to the FF/FFG packages, V_{CCAUX_IO} must be connected to the appropriate voltage/regulator.

Die Level Bank Numbering Overview

Banking and Clocking Summary

- The center clocking backbone contains all vertical clock tracks and clock buffer connectivity.
- The CMT backbone contains all vertical CMT connectivity and is located in the CMT column.
- Not all banks are bonded out in every part/package combination.
- GTP/GTX/GTH columns summary
  - One GT Quad = Four transceivers = Four GTPE2 or GTXE2 or GTHE2 primitives.
  - Not all GT Quads are bonded out in every package.
- I/O banks summary
  - Each bank has four pairs of clock capable (CC) inputs for four differential or four single ended clock inputs.
    - Can connect to the CMT in the same region and the region above and below (with restrictions).
    - Two MRCC pairs can connect to the BUFRs and BUFIOs in the same region/banks and the regions/banks above and below.
    - Two SRCC pairs can only connect to the BUFRs and BUFIOs in the same region/bank.
    - There are no global clock pins (GC pins) in the 7 series FPGAs.
  - Each user I/O bank has 50 single-ended I/Os or 24 differential pairs (48 differential I/Os). The top and bottom I/O pin are always single ended. All 50 pads of a bank are not always bonded out to pins.
- Bank locations of dedicated and dual-purpose pins
  - In most devices, banks 14 and 15 always contain the dual-purpose configuration pins. Bank 15 and 35 contains the XADC auxiliary inputs; however, in Kintex-7 devices, the auxiliary inputs are only in bank 15. Bank 0 contains the dedicated configuration pins.
  - All dedicated configuration I/Os (bank 0) are 3.3V capable
- The physical XY locations for each IDELAYCTRL start at X0Y0 in the bottom left-most bank. The locations then increment by one starting with the lowest bank number in each column in the vertical Y direction and by one for each column in the horizontal X direction. IDELAYCTRLs are located in each of the HROWs.

Figure 1-1 through Figure 1-20 visually describe a die view of the FPGA bank numbering.

Note: The figures for some Virtex-7 HT FPGAs are in development.

XC7A100T Bank

Figure 1-1 shows the I/O and transceiver banks for the XC7A100T.

FTG256 Package

- HR I/O banks 13 and 16 are not bonded out.
- HR I/O bank 34 is partially bonded out.
- The GTP Quads 213 and 216 are not bonded out.

CSG324 Package

- HR I/O bank 13 is not bonded out.
- HR I/O bank 16 is partially bonded out.
- The GTP Quads 213 and 216 are not bonded out.

FGG484 Package

- HR I/O bank 13 is partially bonded out.
- The GTP Quad 213 is not bonded out.

FGG676 Package

- All HR I/O banks and the GTP Quads are fully bonded out in this package.

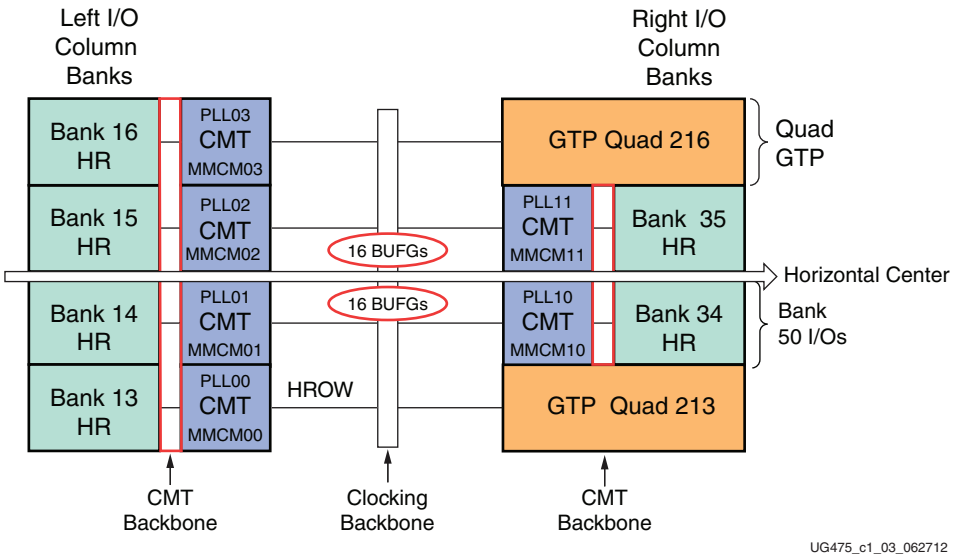

Figure 1-1: **XC7A100T Banks**

XC7A200T Banks

Figure 1-2 shows the I/O and transceiver banks for the XC7A200T.

SBG484 Package

- HR I/O bank 13 is partially bonded out.
- HR I/O banks 12, 32, 33, and 36 are not bonded out.
- The GTP Quads 113, 116, and 213 are not bonded out.

FBG484 Package

- HR I/O bank 13 is partially bonded out.
- HR I/O banks 12, 32, 33, and 36 are not bonded out.
- The GTP Quads 113, 116, and 213 are not bonded out.

FBG676 Package

- HR I/O banks 32 and 36 are not bonded out.
- The GTP Quads 113 and 116 are not bonded out.

FBG1156 Package

- All HR I/O banks and the GTP Quads are fully bonded out in this package.

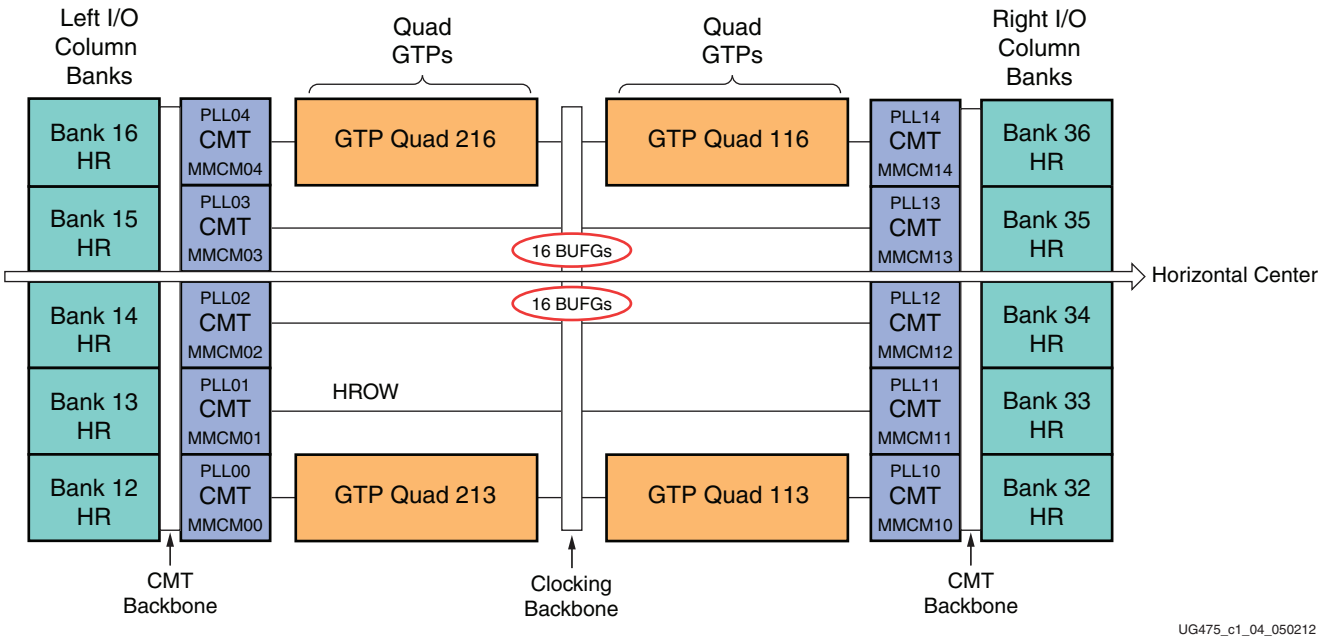

Figure 1-2: **XC7A200T Banks**

XC7K70T Banks

Figure 1-3 shows the I/O and transceiver banks for the XC7K70T.

FBG484 Package

- HR I/O bank 16 is partially bonded out.
- All HP I/O banks are fully bonded out.
- The GTX Quad 116 is not bonded out.

FBG676 Package

- All HR and HP I/O banks and the GTX Quads are fully bonded out in this package.

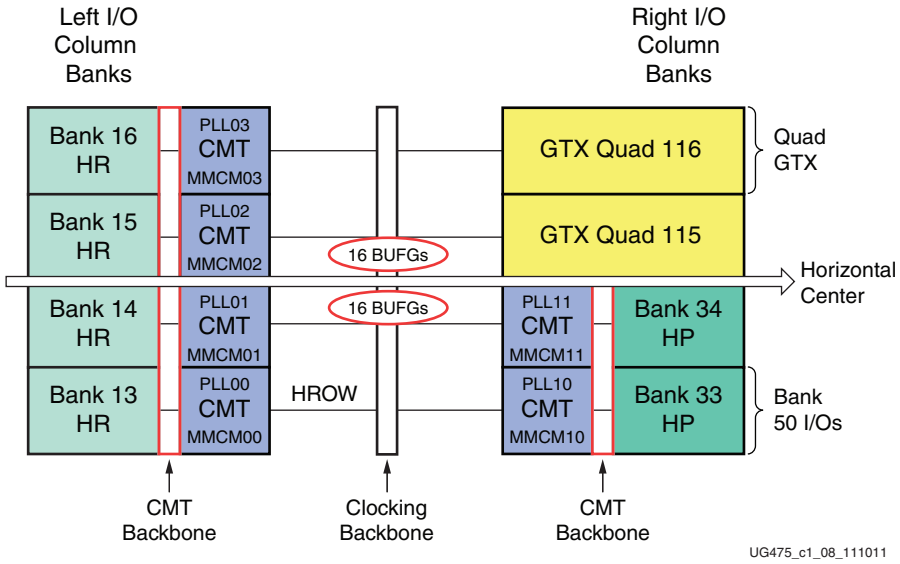

Figure 1-3: **XC7K70T Banks**

XC7K160T Banks

Figure 1-4 shows the I/O and transceiver banks for the XC7K160T.

FBG484 Package

- HR I/O bank 12 is not bonded out and bank 16 is partially bonded out.
- HP I/O bank 32 is not bonded out.
- The GTX Quad 116 is not bonded out.

FBG676 and FFG676 Packages

- All HR and HP I/O banks and the GTX Quads are fully bonded out in these packages.

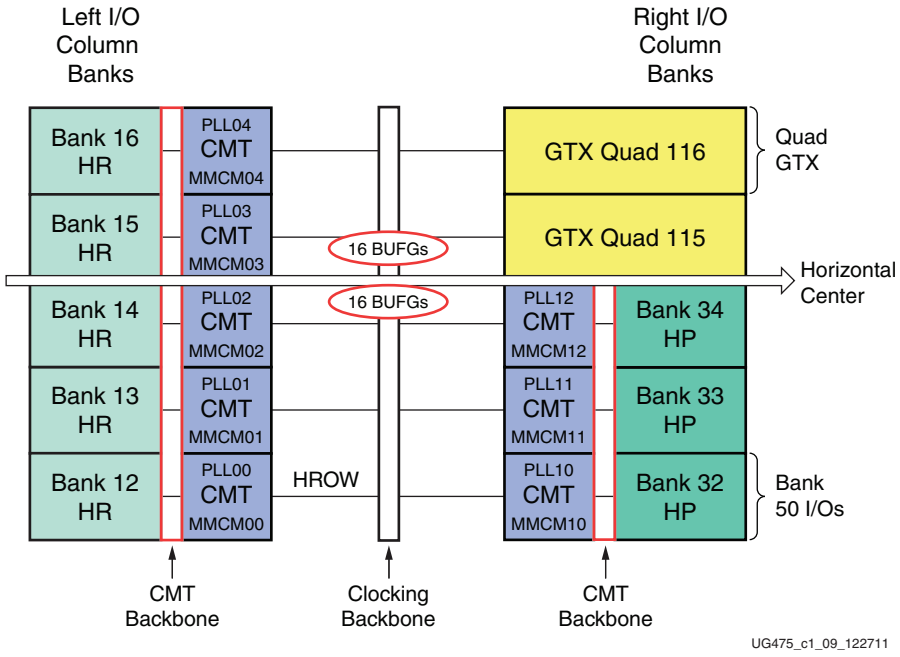

Figure 1-4: **XC7K160T Banks**

XC7K325T Banks

Figure 1-5 shows the I/O and transceiver banks for the XC7K325T.

FBG676 and FFG676 Packages

- HR I/O banks 17 and 18 are not bonded out.
- All HP I/O banks are fully bonded out.
- GTX Quads 117 and 118 are not bonded out.

FBG900 and FFG900 Packages

All HR and HP I/O banks and the GTX Quads are fully bonded out in these packages.

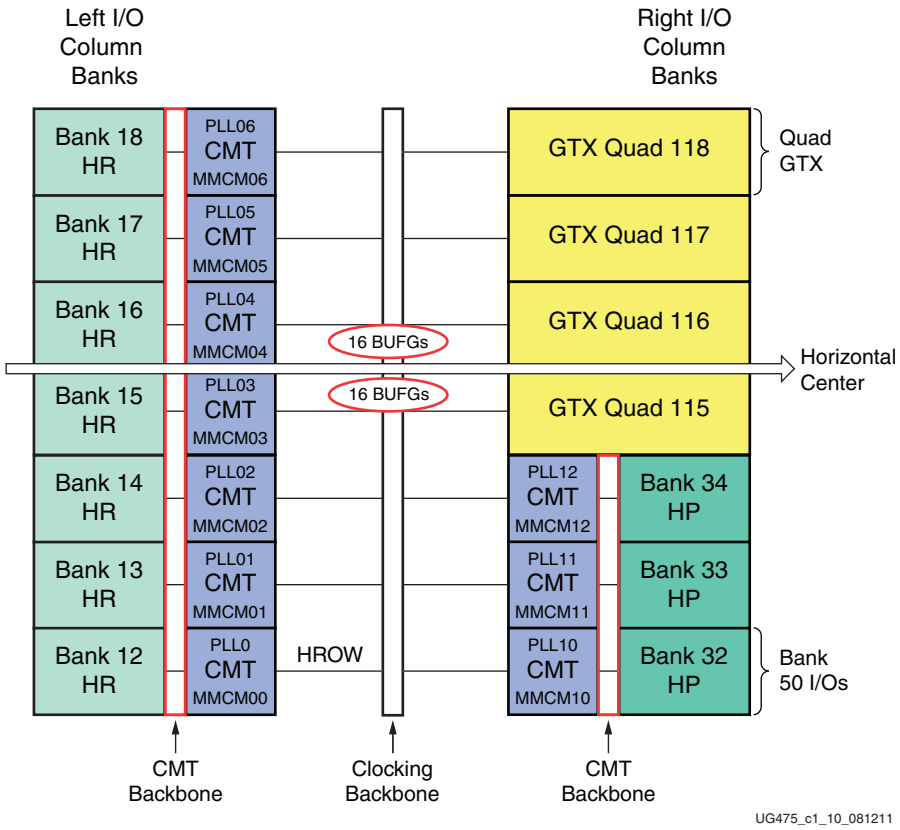

Figure 1-5: **XC7K325T Banks**

XC7K355T Banks

Figure 1-6 shows the I/O and transceiver banks for the XC7K355T.

FFG901 Package

All HR I/O banks and the GTX Quads are fully bonded out in this package.

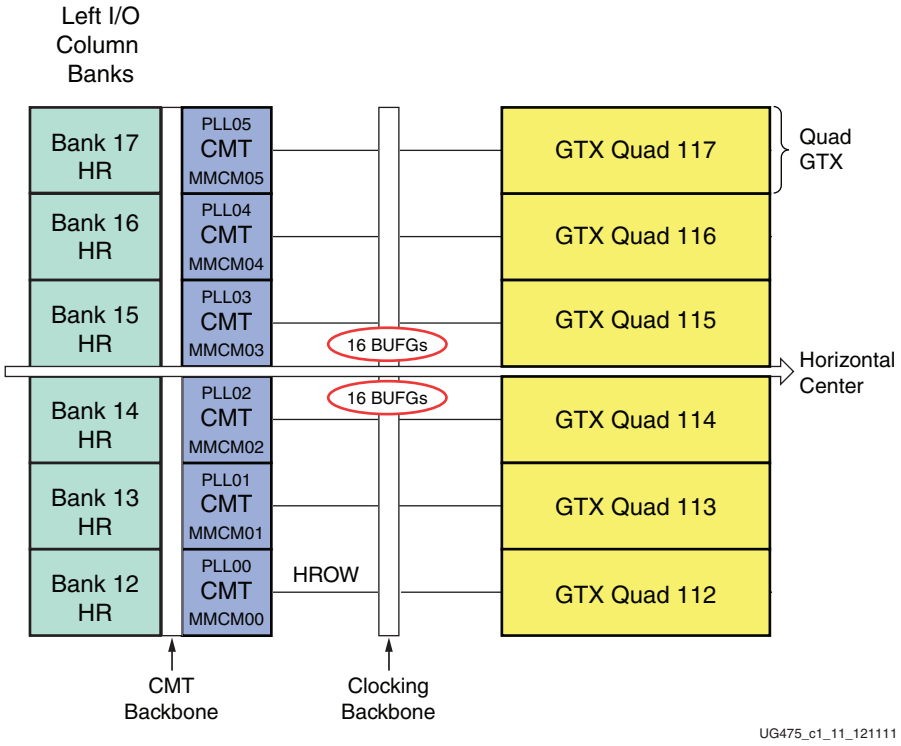

Figure 1-6: **XC7K355T Banks**

XC7K410T Banks

Figure 1-7 shows the I/O and transceiver banks for the XC7K410T.

FBG676 and FFG676 Packages

- HR I/O banks 17 and 18 are not bonded out.
- All HP I/O banks are fully bonded out.
- GTX Quads 117 and 118 are not bonded out.

FBG900 and FFG900 Packages

All HR and HP I/O banks and the GTX Quads are fully bonded out in these packages.

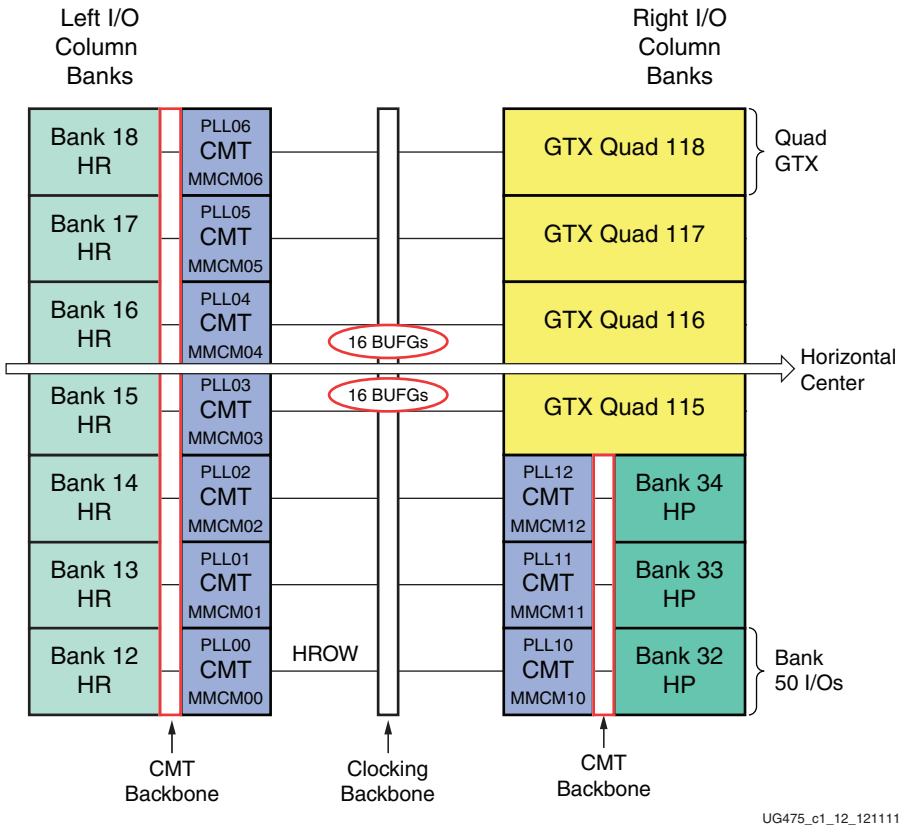

Figure 1-7: **XC7K410T Banks**

XC7K420T Banks

Figure 1-8 shows the I/O and transceiver banks for the XC7K420T.

FFG901 Package

- HR I/O bank 18 is not fully bonded out.
- GTX Quad 118 is not bonded out.

FFG1156 Package

- All HR I/O banks and the GTX Quads are fully bonded out in this package.

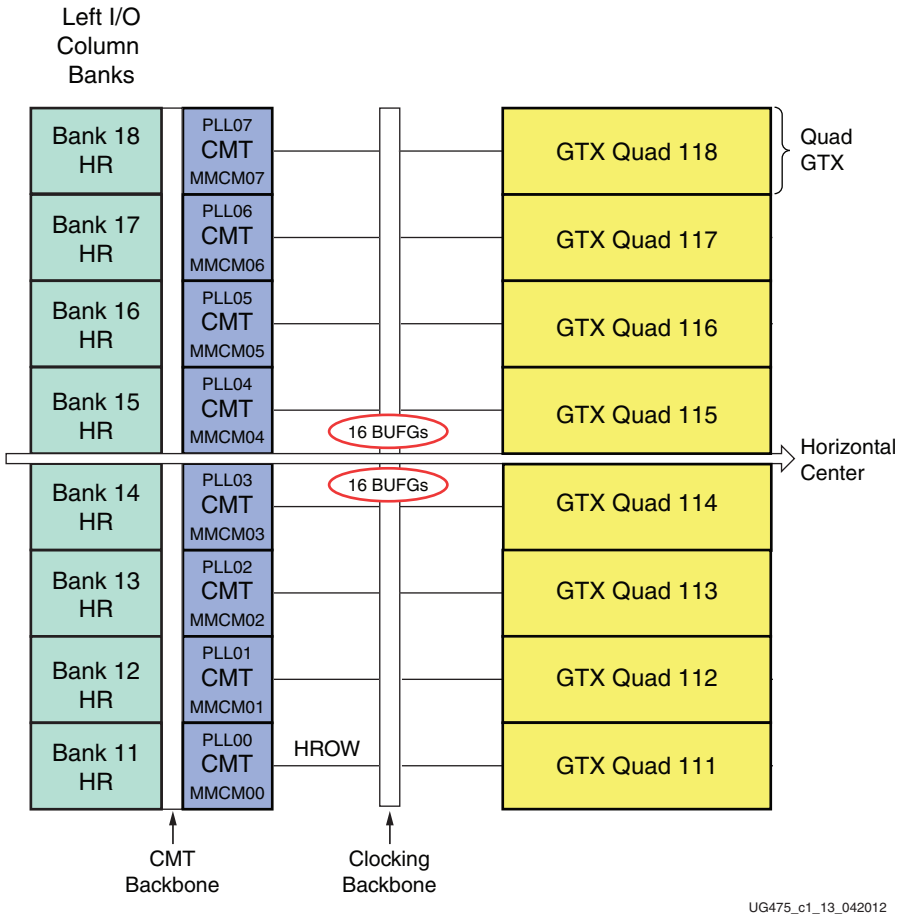

Figure 1-8: **XC7K420T Banks**

XC7K480T Banks

Figure 1-9 shows the I/O and transceiver banks for the XC7K480T.

FFG901 Package

- HR I/O bank 18 is not fully bonded out.
- GTX Quad 118 is not bonded out.

FFG1156 Package

- All HR I/O banks and the GTX Quads are fully bonded out in this package.

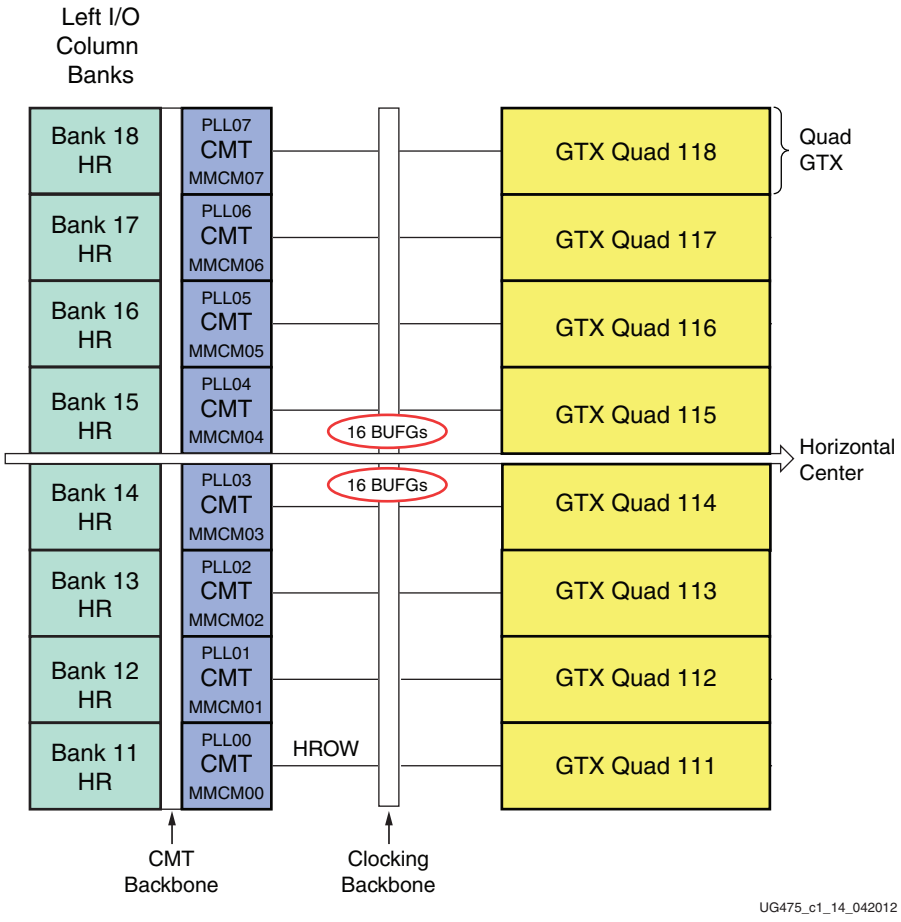

Figure 1-9: **XC7K480T Banks**

XC7V585T Banks

Figure 1-10 shows the I/O and transceiver banks for the XC7V585T.

FFG1157 Package

- All HR I/O banks (11, 12, and 13) are not bonded out.
- HP I/O banks 31, 32, and 33 are not bonded out.
- GTX Quads 111, 112, 113, and 119 are not bonded out.

FFG1761 Package

- HR I/O bank 11 is not bonded out.
- All HP I/O banks and the GTX Quads are fully bonded out in this package.

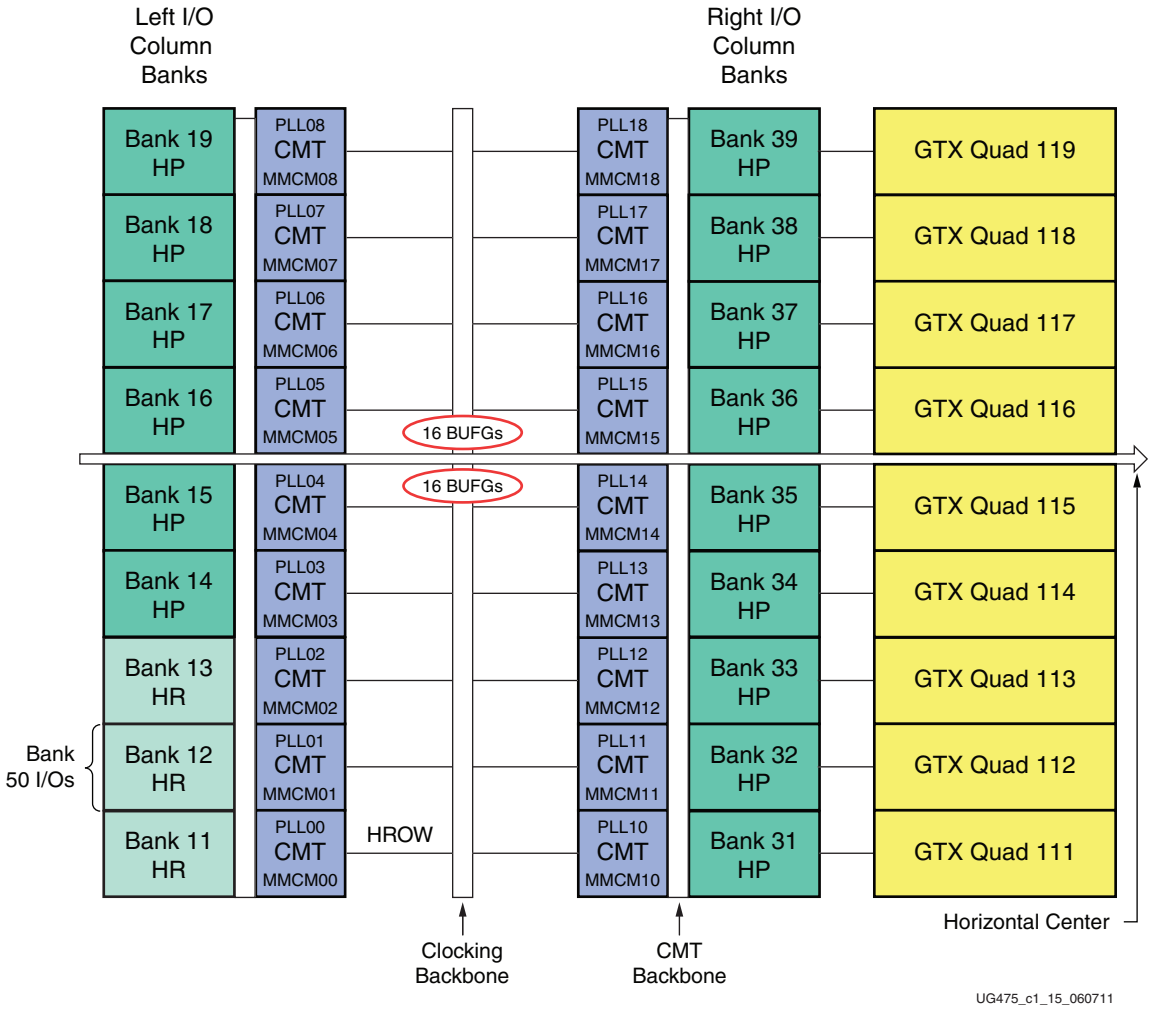

Figure 1-10: **XC7V585T Banks**

XC7V2000T Banks

Figure 1-11 shows the I/O and transceiver banks for the XC7V2000T.

FHG1761 Package

- HP I/O banks 11, 20, 21, 22, 40, 41, and 42 are not bonded out.
- GTX Quads 120, 121, and 122 are not bonded out.

FLG1925 Package

- All HP I/O banks are fully bonded out in this package.
- GTX Quads 111, 116, 117, 118, 119, 120, 121, and 122 are not bonded out.

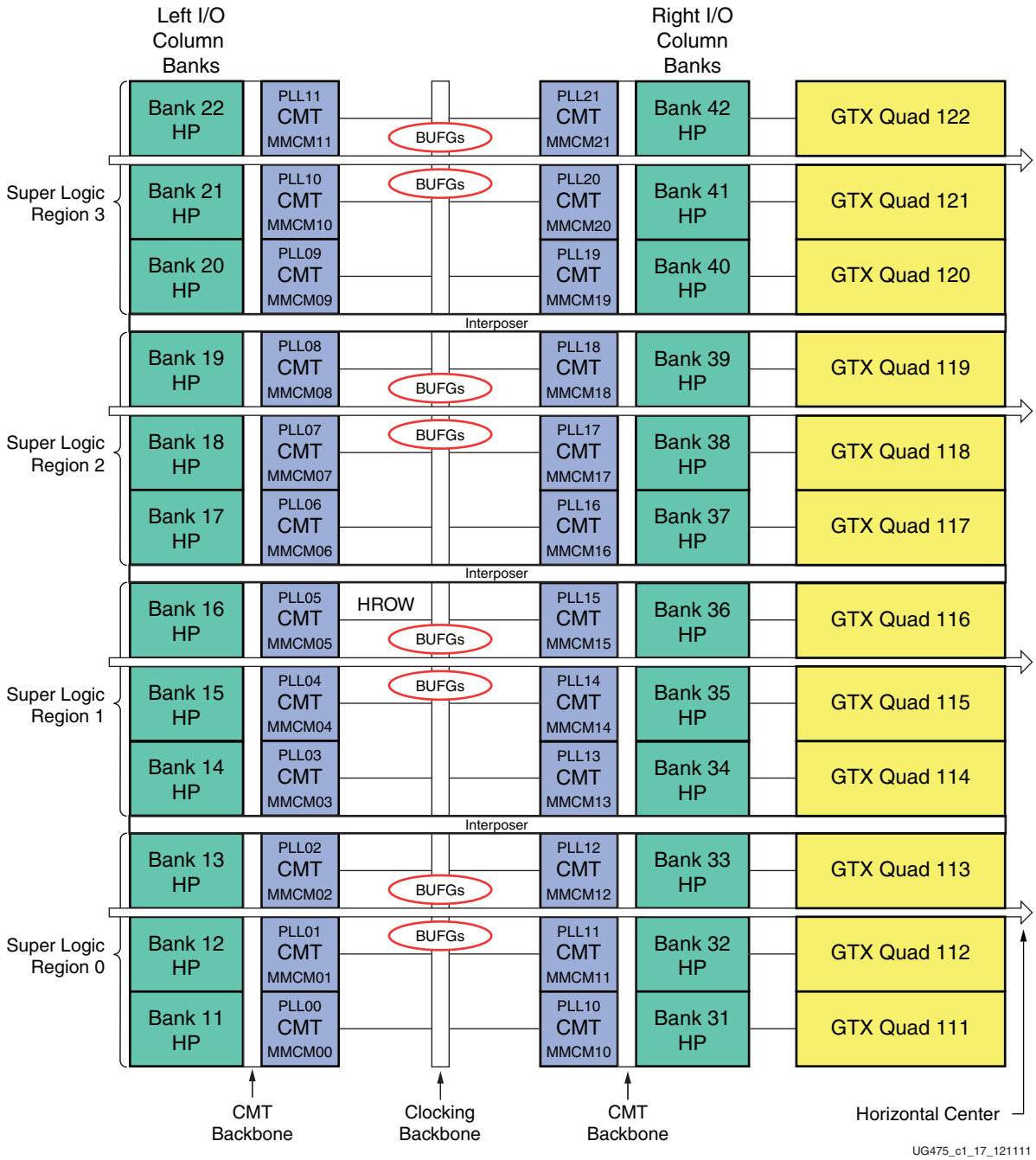

Figure 1-11: **XC7V2000T Banks**

XC7VX330T Banks

Figure 1-12 shows the I/O and transceiver banks for the XC7VX330T.

FFG1157 Package

- HR I/O bank 13 is not bonded out.
- HP I/O bank 33 is not bonded out.
- GTH Quads 113 and 119 are not bonded out.

FFG1761 Package

All HR and HP I/O banks and the GTH Quads are fully bonded out in this package.

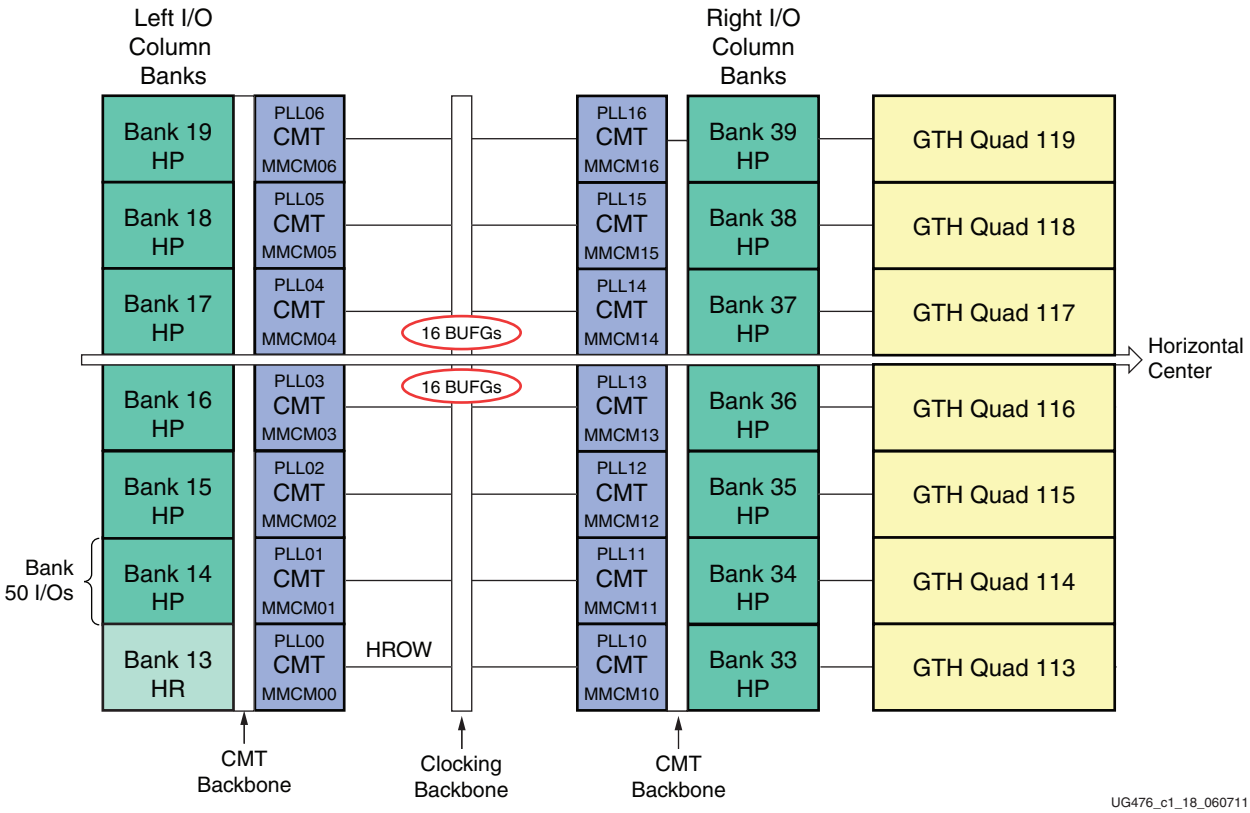

Figure 1-12: **XC7VX330T Banks**

XC7VX415T Banks

Figure 1-13 shows the I/O and transceiver banks for the XC7VX415T.

FFG1157 Package

- All HP I/O banks are fully bonded out.
- GTH Quads 119, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1158 Package

- HP I/O banks 18, 19, 37, 38, and 39 are not bonded out.
- GTH Quads are fully bonded out in this package.

FFG1927 Package

All HP I/O banks and the GTH Quads are fully bonded out in this package.

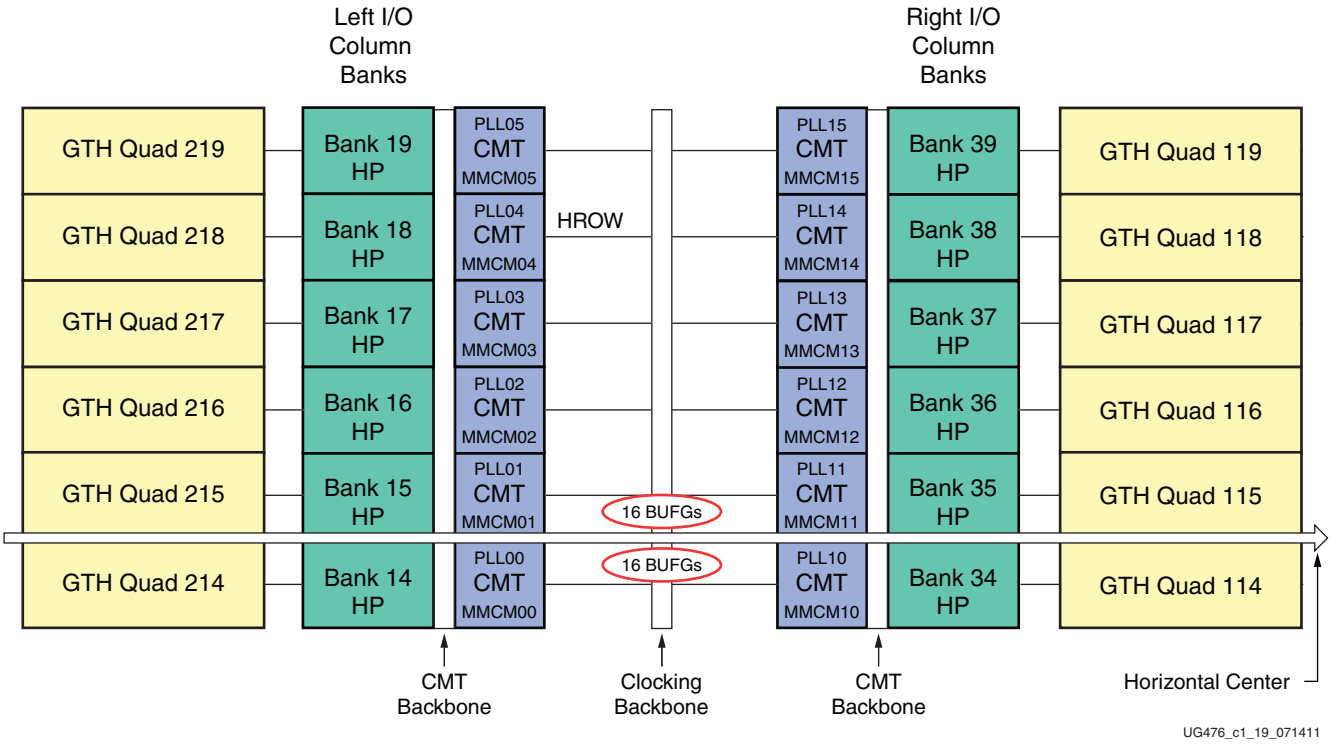

Figure 1-13: **XC7VX415T Banks**

XC7VX485T Banks

Figure 1-14 shows the I/O and transceiver banks for the XC7VX485T.

FFG1157 Package

- HP I/O banks 13 and 33 are not bonded out.
- GTX Quads 113, 119, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1158 Package

- HP I/O banks 13, 18, 19, 33, 37, 38, and 39 are not bonded out.
- GTX Quads 113 and 213 are not bonded out.

FFG1761 Package

- All HP I/O banks are fully bonded out in this package.
- GTX Quads 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1927 Package

- HP I/O banks 13 and 33 are not bonded out.
- All the GTX Quads are fully bonded out in this package.

FFG1930 Package

- All HP I/O banks are fully bonded out in this package.
- GTX Quads 119, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

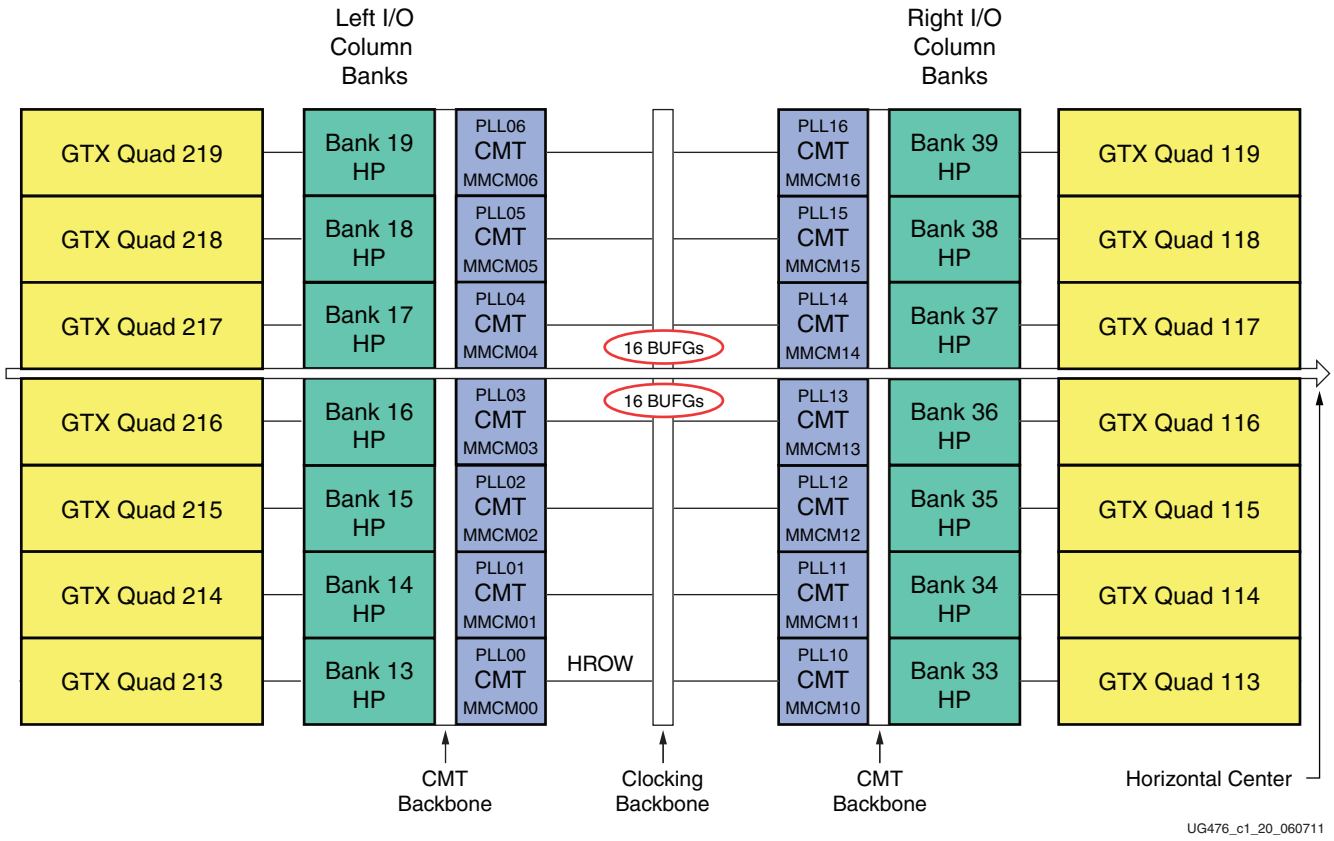

Figure 1-14: **XC7VX485T Banks**

XC7VX550T Banks

Figure 1-15 shows the I/O and transceiver banks for the XC7VX550T.

FFG1158 Package

- HP I/O banks 10, 11, 12, 13, 18, 19, 30, 31, 32, 33, 37, 38, and 39 are not bonded out.
- GTH Quads 110, 111, 112, 113, 210, 211, 212, and 213 are not bonded out.

FFG1927 Package

- HP I/O banks 10, 11, 12, 13, 30, 31, 32, and 33 are not bonded out.
- All GTH Quads are fully bonded out in this package.

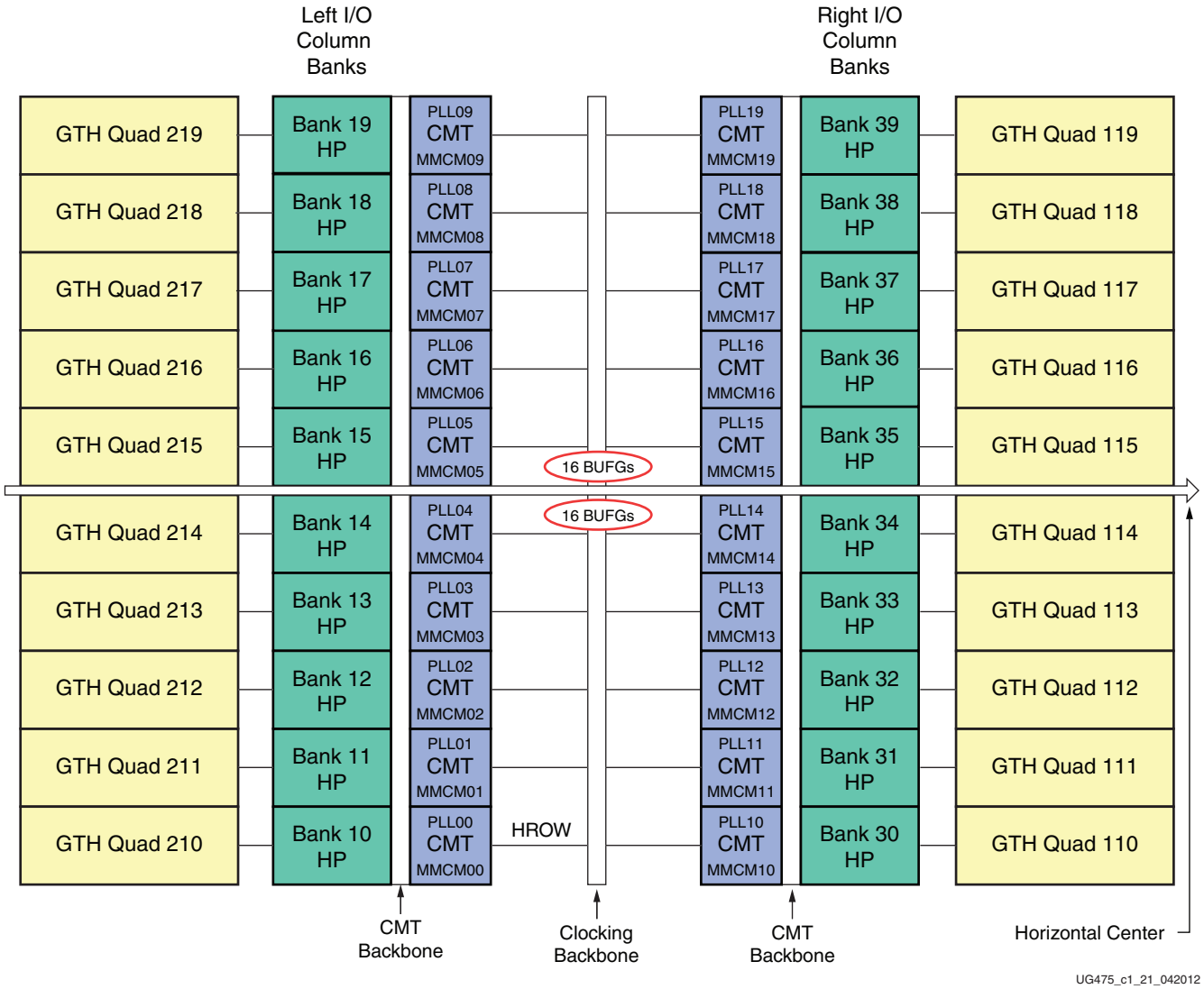

Figure 1-15: **XC7VX550T Banks**

XC7VX690T Banks

Figure 1-16 shows the I/O and transceiver banks for the XC7VX690T.

FFG1157 Package

- HP I/O banks 10, 11, 12, 13, 30, 31, 32, and 33 are not bonded out.
- GTH Quads 110, 111, 112, 113, 119, 210, 211, 212, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1158 Package

- HP I/O banks 10, 11, 12, 13, 18, 19, 30, 31, 32, 33, 37, 38, and 39 are not bonded out.
- GTH Quads 110, 111, 112, 113, 210, 211, 212, and 213 are not bonded out.

FFG1761 Package

- HP I/O banks 10, 11, and 30 are not bonded out.
- GTH Quads 110, 210, 211, 212, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1926 Package

- HP I/O bank 17 is partially bonded out.
- HP I/O banks 18, 19, 37, 38, and 39 are not bonded out.
- GTH Quads 110, 119, 210, and 219 are not bonded out.

FFG1927 Package

- HP I/O banks 10, 11, 12, 13, 30, 31, 32, and 33 are not bonded out.
- All GTH Quads are fully bonded out in this package.

FFG1930 Package

- All HP I/O banks are fully bonded out in this package.
- GTH Quads 110, 111, 112, 119, 210, 211, 212, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

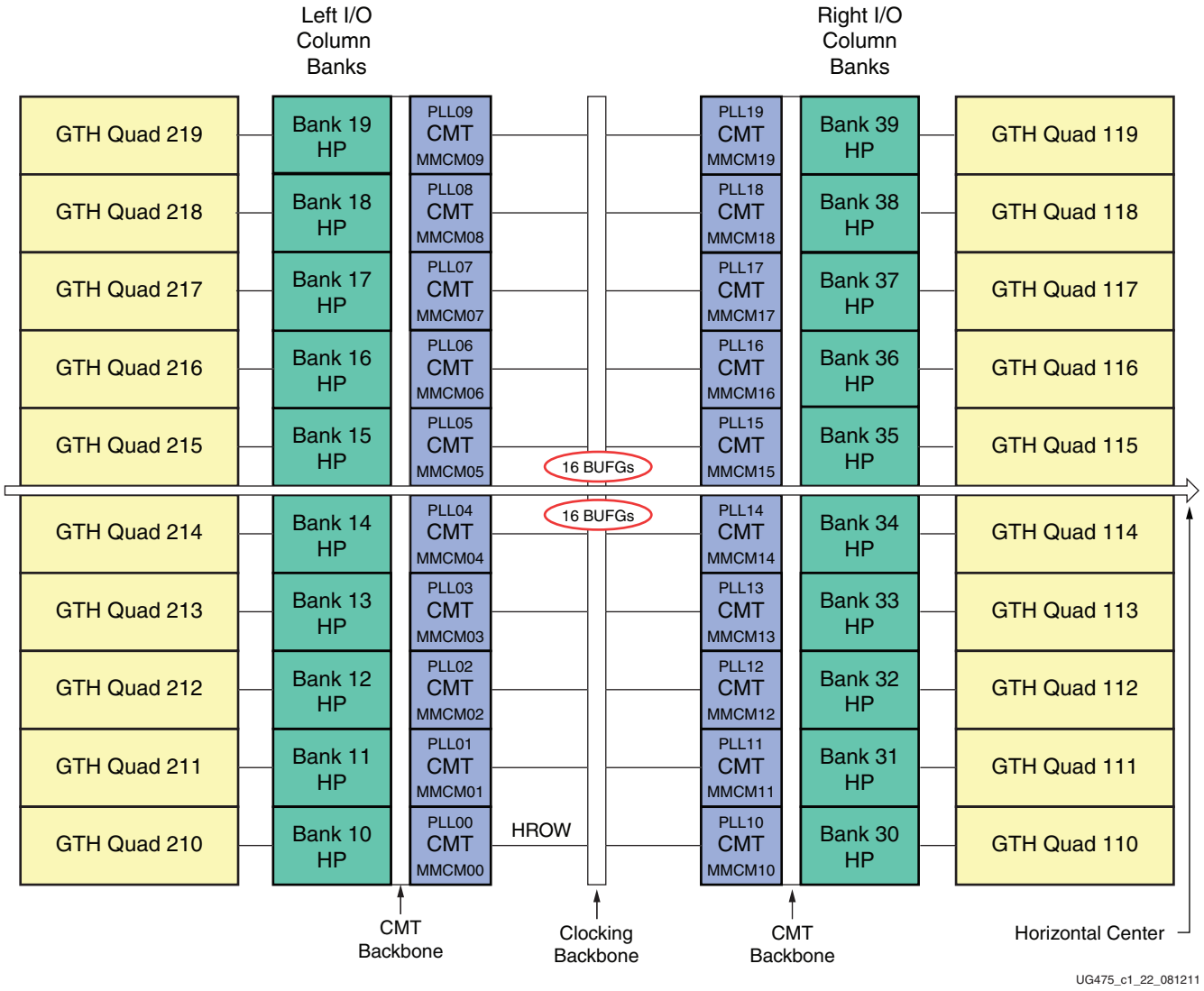

Figure 1-16: **XC7VX690T Banks**

XC7VX980T Banks

Figure 1-17 shows the I/O and transceiver banks for the XC7VX980T.

FFG1926 Package

- HP I/O bank 17 is partially bonded out.
- HP I/O banks 18, 37, and 38 are not bonded out.
- GTH Quads 110 and 210 are not bonded out.

FFG1928 Package

- HP I/O bank 16 is partially bonded out.
- HP I/O banks 10, 11, 12, 17, 18, 30, 31, and 32 are not bonded out.
- All GTH Quads are fully bonded out in this package.

FFG1930 Package

- All HP I/O banks are fully bonded out in this package.
- GTH Quads 110, 111, 112, 210, 211, 212, 213, 214, 215, 216, 217, and 218 are not bonded out.

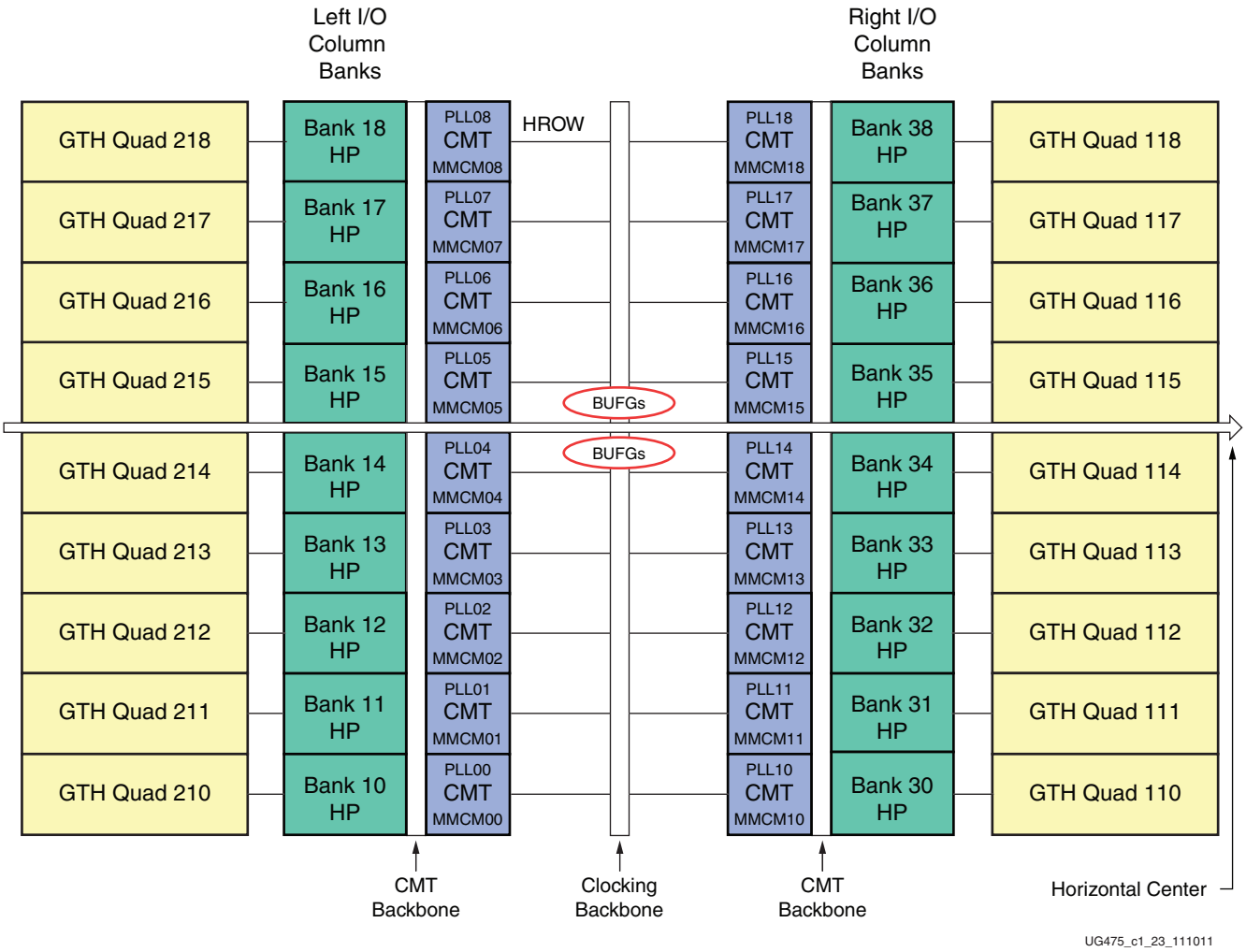

Figure 1-17: **XC7VX980T Banks**

XC7VX1140T Banks

Figure 1-18 shows the I/O and transceiver banks for the XC7VX1140T.

FLG1926 Package

- HP I/O bank 17 is partially bonded out.
- HP I/O banks 18, 19, 20, 21, 37, 38, 39, 40, and 41 are not bonded out.
- GTH Quads 110, 119, 120, 121, 210, 219, 220, and 221 are not bonded out.

FLG1928 Package

- HP I/O bank 16 is partially bonded out.
- HP I/O banks 10, 11, 12, 17, 18, 19, 20, 21, 30, 31, 32, 39, 40, and 41 are not bonded out.
- All GTH Quads are fully bonded out in this package.

FLG1930 Package

- HP I/O banks 40 and 41 are not bonded out.
- GTH Quads 110, 111, 112, 119, 120, 121, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, and 221 are not bonded out.

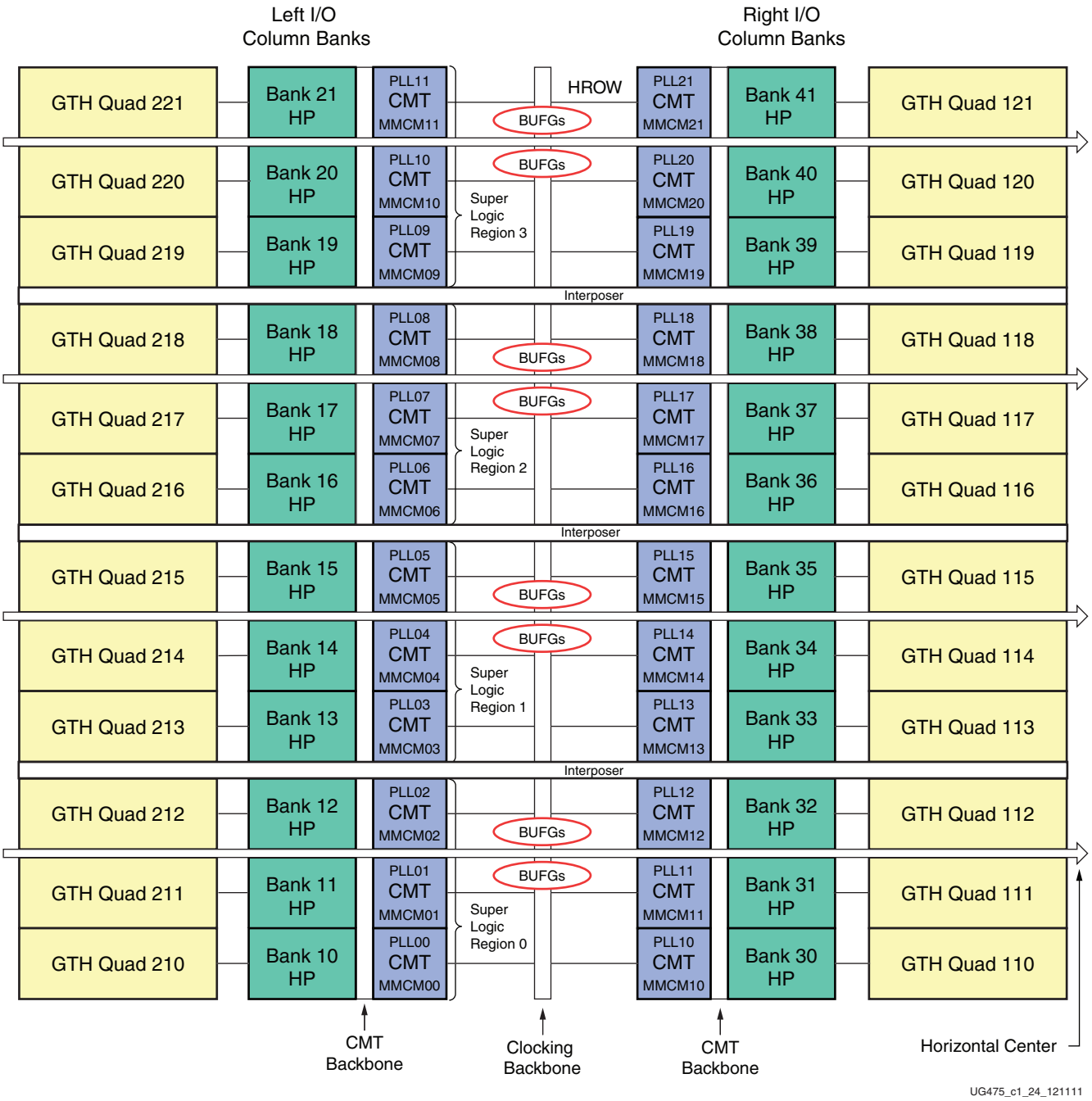

Figure 1-18: **XC7VX1140T Banks**

XC7VH580T Banks

Figure 1-19 shows the I/O and transceiver banks for the XC7VH580T.

HCG1155 Package

- HP I/O banks 17, 18, 37, and 38 are not bonded out.
- GTH Quads 116, 117, 118, 216, 217, and 218 are not bonded out.
- The GTZ Octal 300 is fully bonded out in this package.

HCG1931 Package

- All HP I/O banks are fully bonded out in this package.
- All GTH Quads are fully bonded out in this package.
- The GTZ Octal 300 is fully bonded out in this package.

HCG1932 Package

- HP I/O banks 16, 17, 18, 36, 37, and 38 are not bonded out in this package.
- All GTH Quads are fully bonded out in this package.
- The GTZ Octal 300 is fully bonded out in this package.

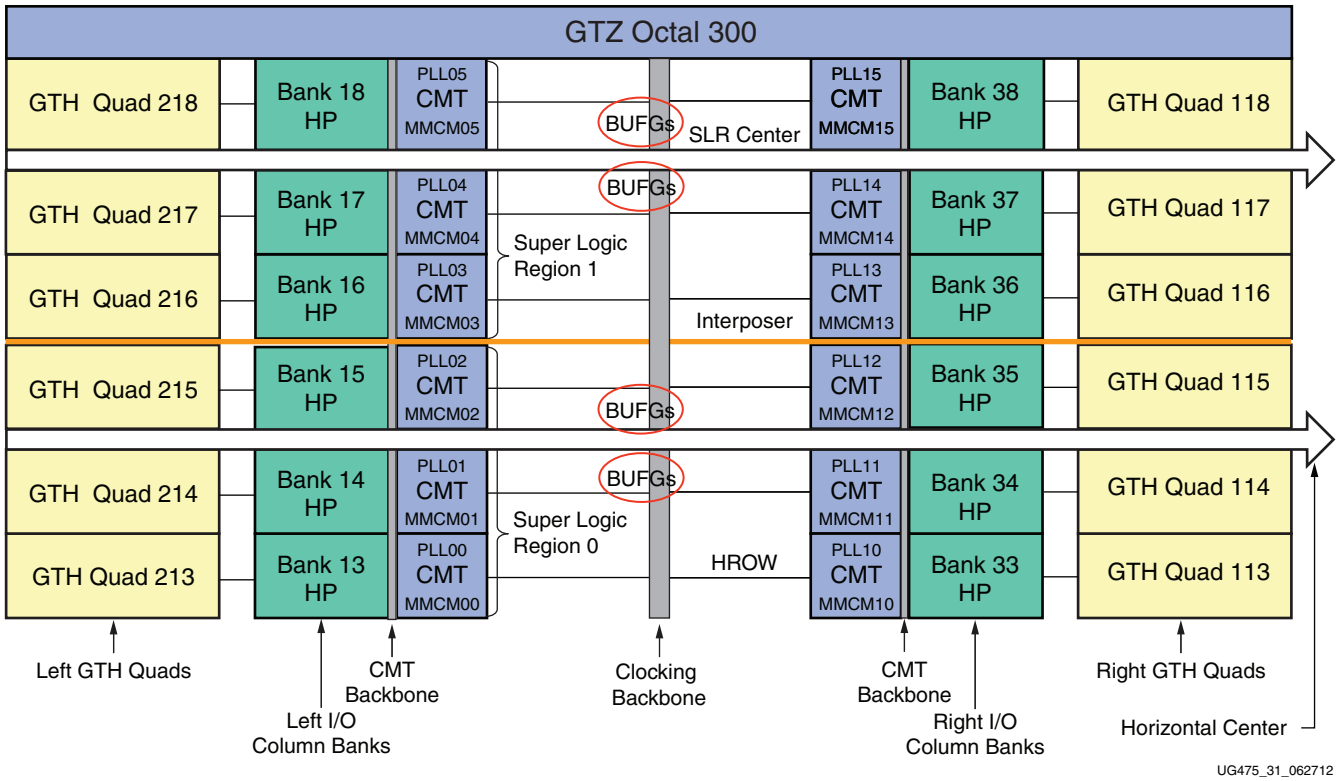

Figure 1-19: **XC7VH580T Banks**

XC7VH870T Banks

Figure 1-20 shows the I/O and transceiver banks for the XC7VH870T.

HCG1931 Package

- HP I/O banks 10, 11, 12, 30, and 31 are not bonded out.
- GTH Quads 110, 111, 112, 210, 211, and 212 are not bonded out.
- The GTZ Octal 400 is not bonded out in this package.

HCG1932 Package

- HP I/O banks 10, 11, 12, 16, 17, 18, 30, 31, 32, 36, 37, and 38 are not bonded out in this package.
- All GTH Quads are fully bonded out in this package.
- Both GTZ Octals are fully bonded out in this package.

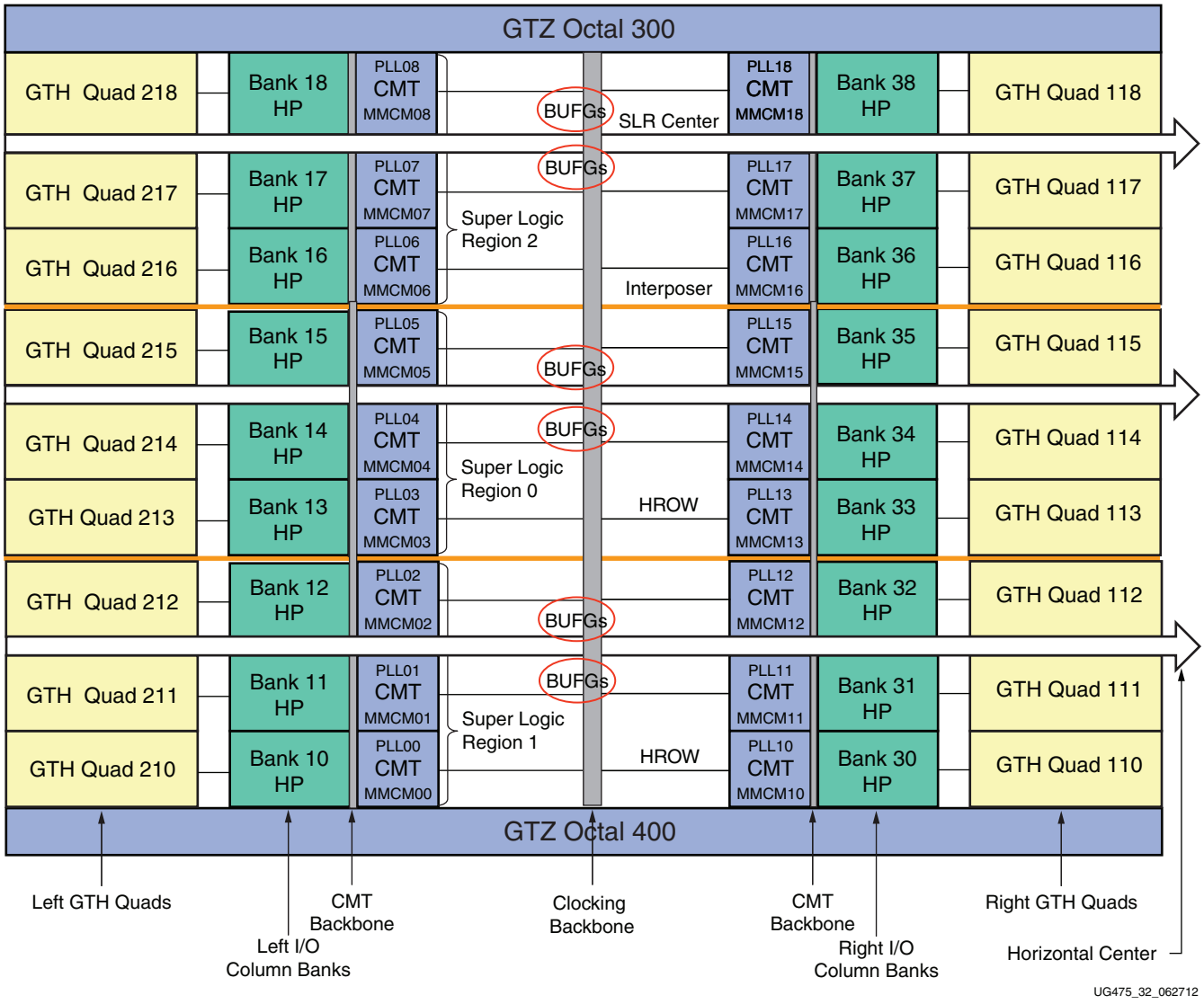

Figure 1-20: **XC7VH870T Banks**

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Chapter 2

7 Series FPGAs Package Files

About ASCII Package Files

The ASCII files for each package include a comma-separated-values (CSV) version and a text version optimized for a browser or text editor. Each of the files consists of the following:

- Device/Package name (*FPGA Family—Device—Package*), date and time of creation
- Eight columns containing data for each pin:
  - Pin—Pin location on the package.
  - Pin Name—The name of the assigned pin.
  - Memory Byte Group—Memory byte group between 0 and 3. For more information on the memory byte group, see UG586, *7 Series FPGAs Memory Interface Solutions User Guide*.
  - Bank—Bank number.
  - V_{CCAUX} Group—Number corresponding to the V_{CCAUX_IO} power supply for the given pin. V_{CCAUX} is shown for packages with only one V_{CCAUX} group.
  - Super Logic Region—Number corresponding to the super logic region (SLR) in the devices implemented with stacked silicon interconnect (SSI) technology.
  - I/O Type—CONFIG, HR, HP, or GT (GTP, GTX, GTH, GTZ) depending on the I/O type. For more information on the I/O type, see UG471, *7 Series FPGAs SelectIO Resources User Guide*.
  - No-Connect—This list of devices is used for migration between devices that have the same package size and are not connected at that specific pin.
- Total number of pins in the package.

ASCII Pinout Files

This chapter includes the pinout information tables for the following device/packages.

Note: All package files are ASCII files in TXT and CSV file format.

To download all available Artix-7 FPGAs package/device/pinout files click here:

http://www.xilinx.com/support/packagefiles/artix-7-pkgs.htm

Note: Only the available files listed in Table 2-1 are linked and consolidated in the above ZIP file.

Table 2-1: **Artix-7 FPGAs Package/Device Pinout Files**

Device	CSG324	FTG256	SBG484	FGG484	FGG676	FBG484	FBG676	FFG1156
XC7A100T	CSG324	FTG256		FGG484	FGG676			
XC7A200T			SBG484			FBG484	FBG676	FFG1156

To download all available Kintex-7 FPGAs package/device/pinout files click here:

http://www.xilinx.com/support/packagefiles/kintex-7-pkgs.htm

Table 2-2: **Kintex-7 FPGAs Package/Device Pinout Files**

Device	FB484/ FBG484	FB676/ FBG676	FB900/ FBG900	FF676/ FFG676	FF900/ FFG900	FF901/ FFG901	FF1156/ FFG1156
XC7K70T	FBG484	FBG676					
XC7K160T	FB484/ FBG484	FB676/ FBG676		FF676/ FFG676			
XC7K325T		FB676/ FBG676	FB900/ FBG900	FF676/ FFG676	FF900/ FFG900		
XC7K355T						FF901/ FFG901	
XC7K410T		FB676/ FBG676	FB900/ FBG900	FF676/ FFG676	FF900/ FFG900		
XC7K420T						FF901/ FFG901	FF1156/ FFG1156
XC7K480T						FF901/ FFG901	FF1156/ FFG1156

To download all available Virtex-7 FPGAs package/device/pinout files click here:

http://www.xilinx.com/support/packagefiles/virtex-7-pkgs.htm

Note: Only the available files listed in Table 2-3, Table 2-4, and Table 2-5 are linked and consolidated in the above ZIP file.

Table 2-3: **Virtex-7 T FPGAs Package/Device Pinout Files**

Device	FF1157/FFG1157	FF1761/FFG1761	FL1925/FLG1925	FH1761/FHG1761
XC7V585T	FF1157/FFG1157	FF1761/FFG1761		
XC7V2000T			FL1925/FLG1925	FH1761/FHG1761

Table 2-4: **Virtex-7 XT FPGAs Package/Device Pinout Files**

Device	FF1157/ FFG1157	FF1158/ FFG1158	FF1761/ FFG1761	FF1926/ FFG1926	FF1927/ FFG1927	FF1928/ FFG1928	FF1930/ FFG1930	FL1926/ FLG1926	FL1928/ FLG1928	FL1930/ FLG1930
XC7VX330T	FF1157/ FFG1157		FF1761/ FFG1761							
XC7VX415T	FF1157/ FFG1157	FF1158/ FFG1158			FF1927/ FFG1927					
XC7VX485T	FF1157/ FFG1157	FF1158/ FFG1158	FF1761/ FFG1761		FF1927/ FFG1927		FF1930/ FFG1930			
XC7VX550T		FF1158/ FFG1158			FF1927/ FFG1927					
XC7VX690T	FF1157/ FFG1157	FF1158/ FFG1158	FF1761/ FFG1761	FF1926/ FFG1926	FF1927/ FFG1927		FF1930/ FFG1930			
XC7VX980T				FF1926/ FFG1926		FF1928/ FFG1928	FF1930/ FFG1930			
XC7VX1140T								FL1926/ FLG1926	FL1928/ FLG1928	FL1930/ FLG1930

Table 2-5: **Virtex-7 HT FPGAs Package/Device Pinout Files**

Device	HCG1155	HCG1931	HCG1932
XC7VH580T	HCG1155	HCG1931	HCG1932
XC7VH870T		HCG1931	HCG1932

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Chapter 3

Device Diagrams

Summary

This chapter provides pinout, high-performance and high-range I/O bank, memory groupings, and power and ground placement diagrams for each 7 series FPGA package/device combination.

- Artix-7 FPGAs Device Diagrams, page 57
- Kintex-7 FPGAs Device Diagrams, page 81
- Virtex-7 FPGAs Device Diagrams, page 113

The figures provide a top-view perspective.

The symbols for the multi-function I/O pins are represented by only one of the available pin functions; with precedence (by functionality) in this order:

- ADV_B, FCS_B, FOE_B, MOSI, FWE_B, DOUT_CSO_B, CSI_B, PUDC_B, or RDWR_B
- RS0–RS1
- AD0P/AD0N–AD15P/AD15N
- EMCCLK
- VRN, VRP, or VREF
- D00–D31
- A00–A28
- DQS, MRCC, or SRCC

For example, a pin description such as IO_L8P_SRCC_12 is represented with a SRCC symbol, a pin description such as IO_L19N_T3_A09_D25_VREF_14 is represented with a VREF symbol, and a pin description such as IO_L21N_T3_DQS_A06_D22_14 is represented with a D0–D31 symbol.

Note: The available files are listed in Table 3-1, Table 3-2, Table 3-3, Table 3-4, and Table 3-5 are linked.

Artix-7 FPGAs Device Diagrams

Table 3-1: **Artix-7 FPGAs Device Diagrams Cross-Reference**

Device	CSG324	FTG256	SBG484	FGG484	FGG676	FBG484	FBG676	FFG1156
XC7A100T	page 58	page 60		page 62	page 65			
XC7A200T			page 68			page 71	page 74	page 77

CSG324 Package—XC7A100T

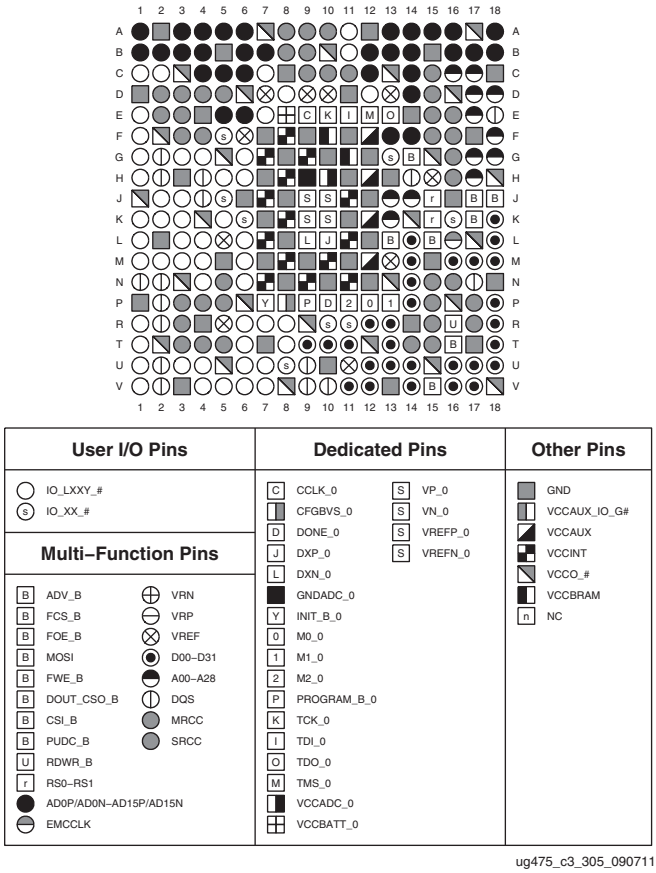

Figure 3-1: **CSG324 Package—XC7A100T Pinout Diagram**

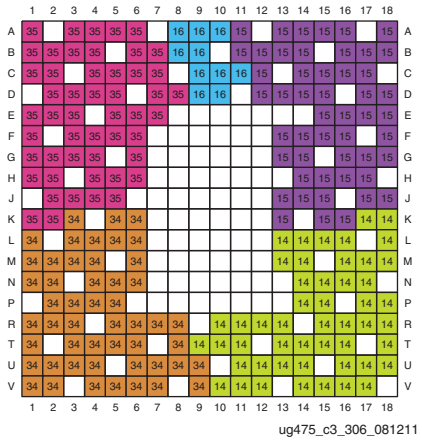

Figure 3-2: **CSG324 Package—XC7A100T I/O Banks**

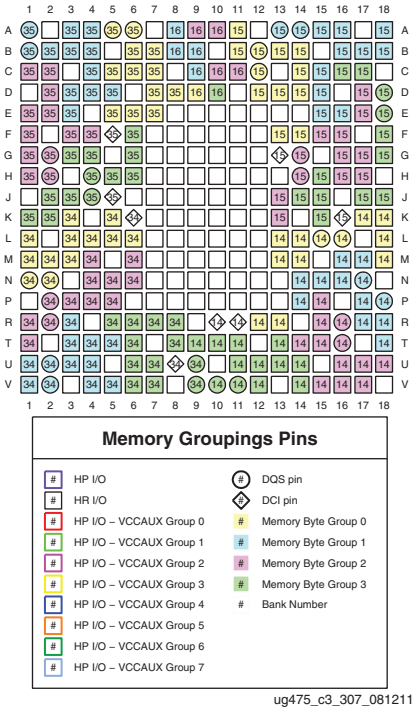

Figure 3-3: **CSG324 Package—XC7A100T Memory Groupings**

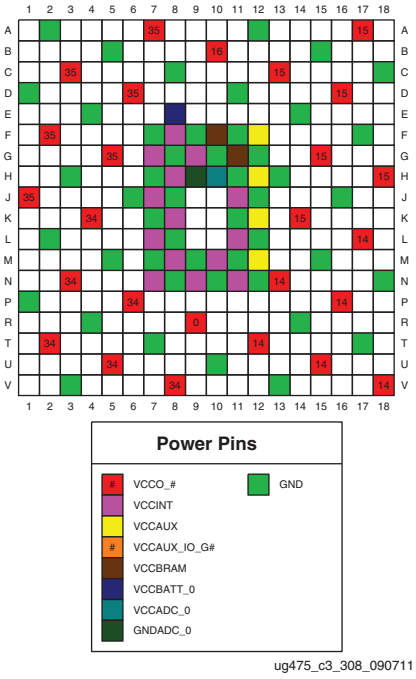

Figure 3-4: **CSG324 Package—XC7A100T Power and GND Placement**

FTG256 Package—XC7A100T

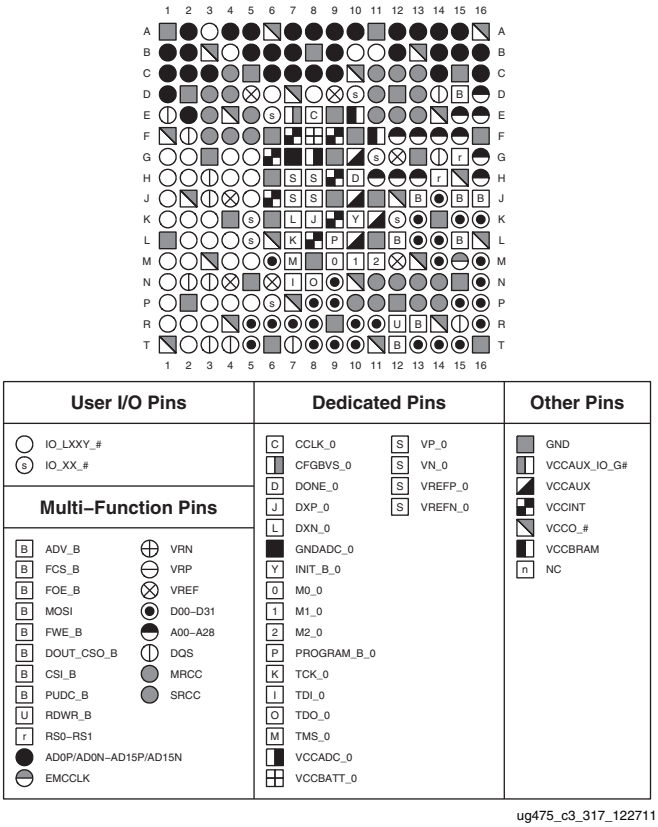

Figure 3-5: **FTG256 Package—XC7A100T Pinout Diagram**

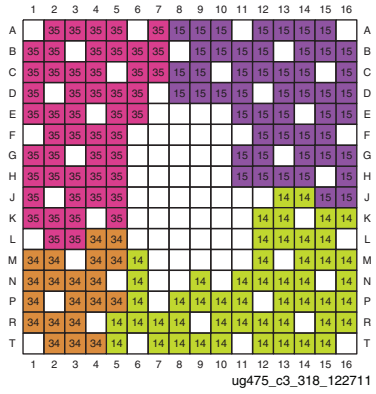

Figure 3-6: **FTG256 Package—XC7A100T I/O Banks**

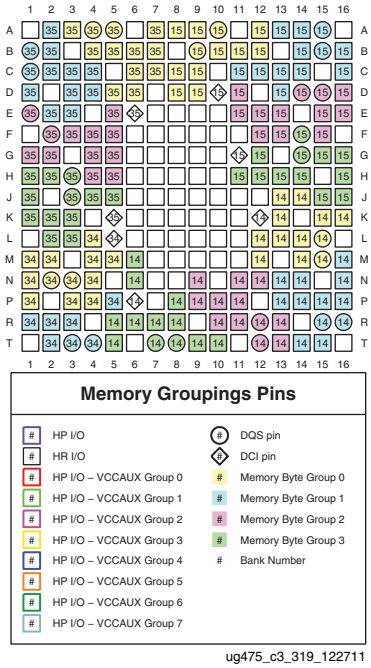

Figure 3-7: **FTG256 Package—XC7A100T Memory Groupings**

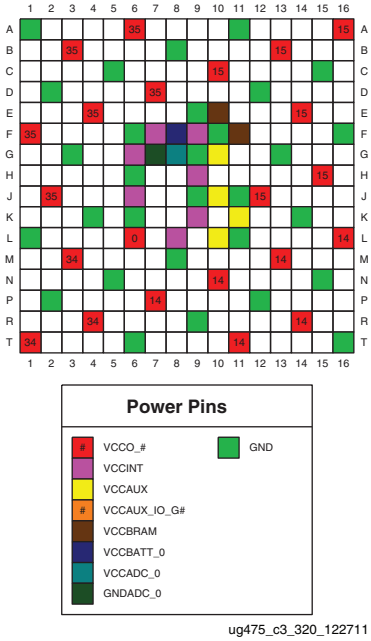

Figure 3-8: **FTG256 Package—XC7A100T Power and GND Placement**

FGG484 Package—XC7A100T

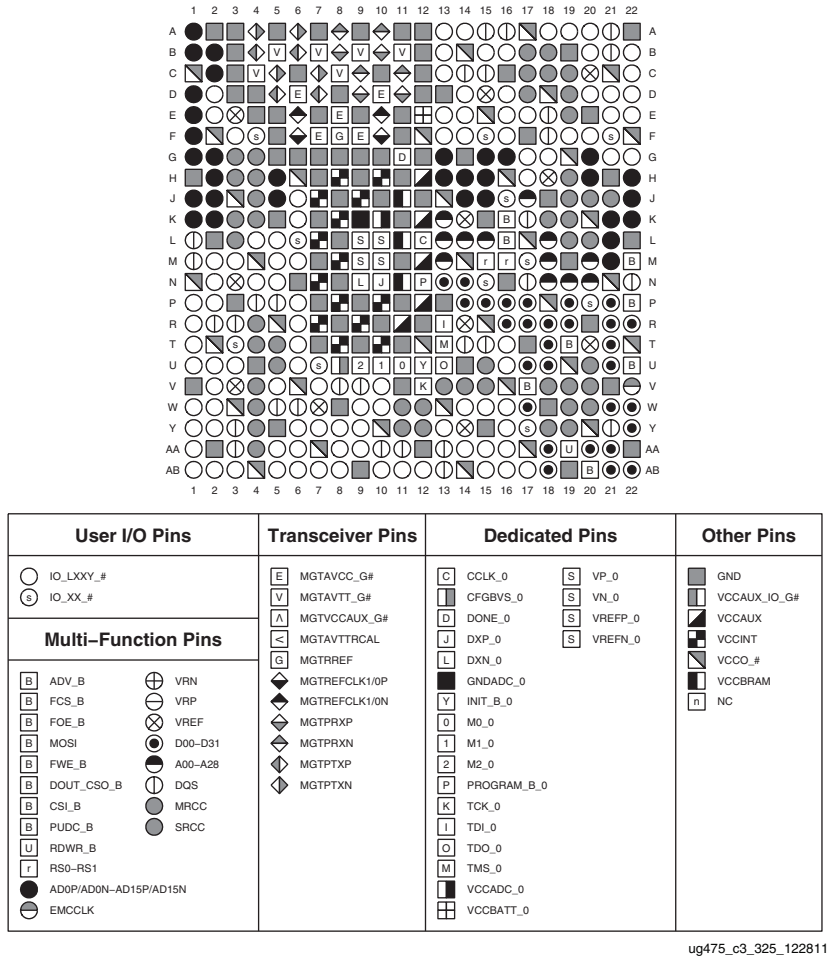

Figure 3-9: **FGG484 Package—XC7A100T Pinout Diagram**

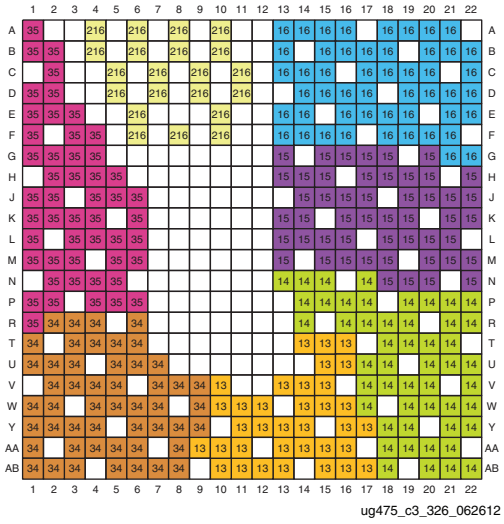

Figure 3-10: **FGG484 Package—XC7A100T I/O Banks**

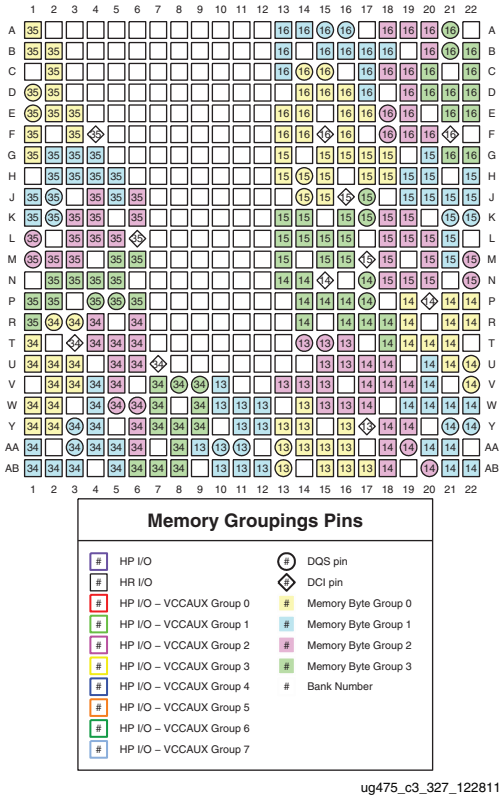

Figure 3-11: **FGG484 Package—XC7A100T Memory Groupings**

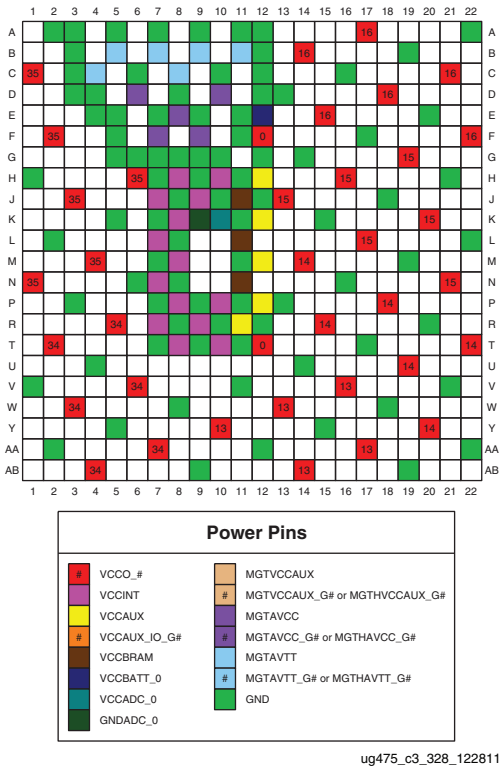

Figure 3-12: **FGG484 Package—XC7A100T Power and GND Placement**

FGG676 Package—XC7A100T

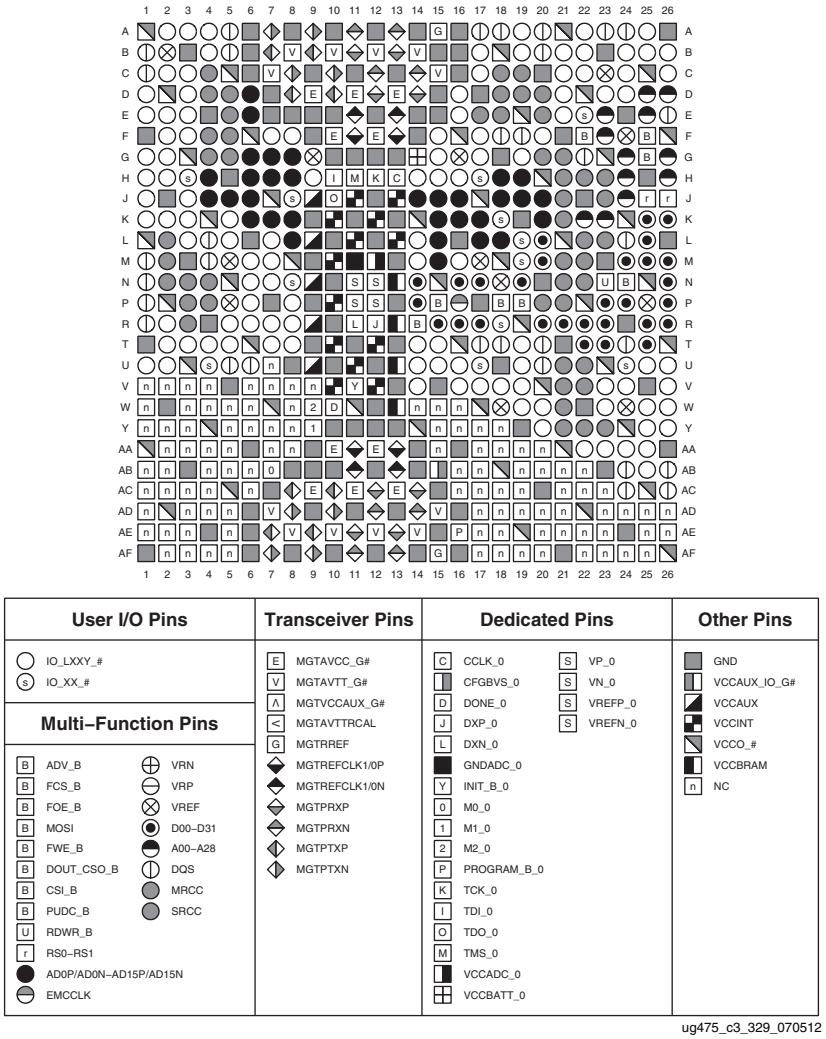

Figure 3-13: **FGG676 Package—XC7A100T Pinout Diagram**

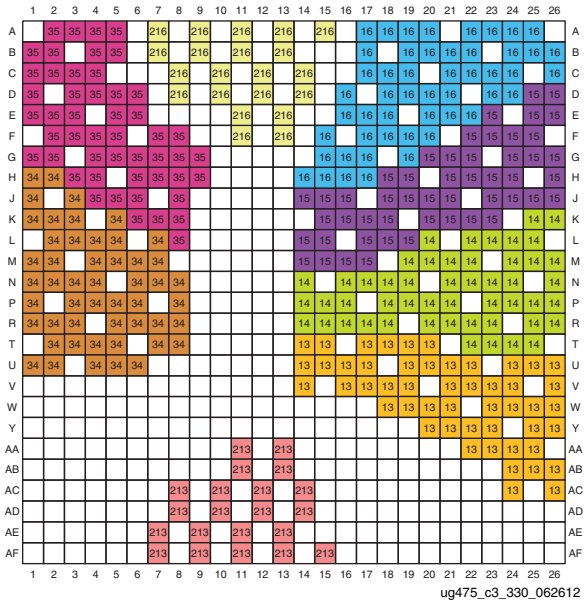

Figure 3-14: **FGG676 Package—XC7A100T I/O Banks**

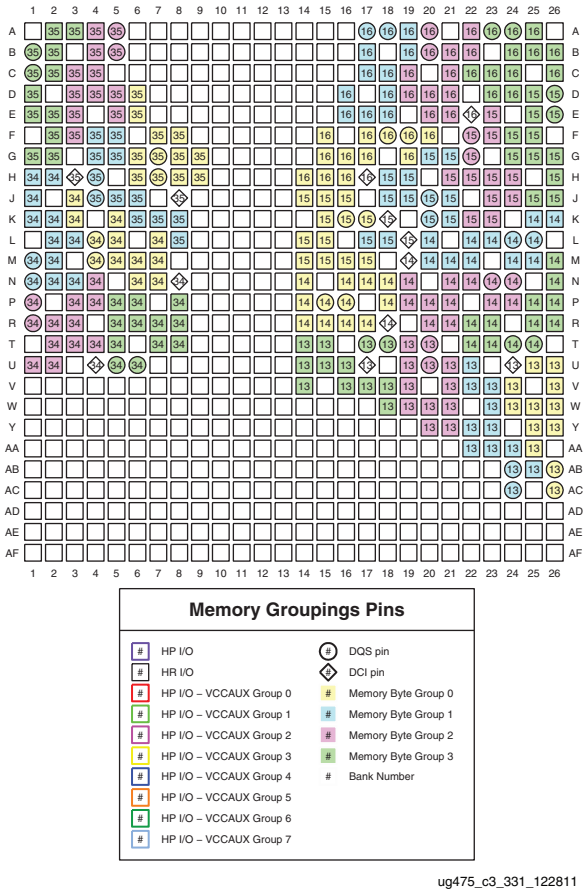

Figure 3-15: **FGG676 Package—XC7A100T Memory Groupings**

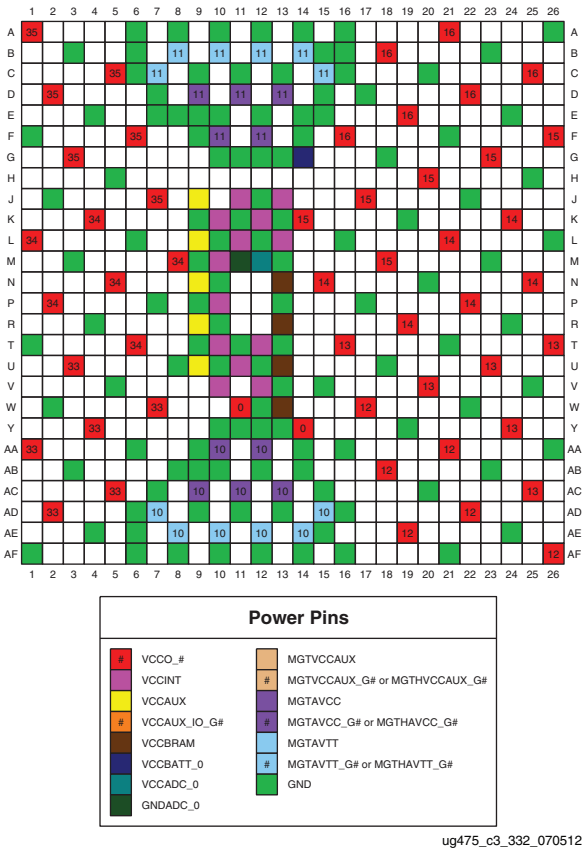

Figure 3-16: **FGG676 Package—XC7A100T Power and GND Placement**

SBG484 Package—XC7A200T

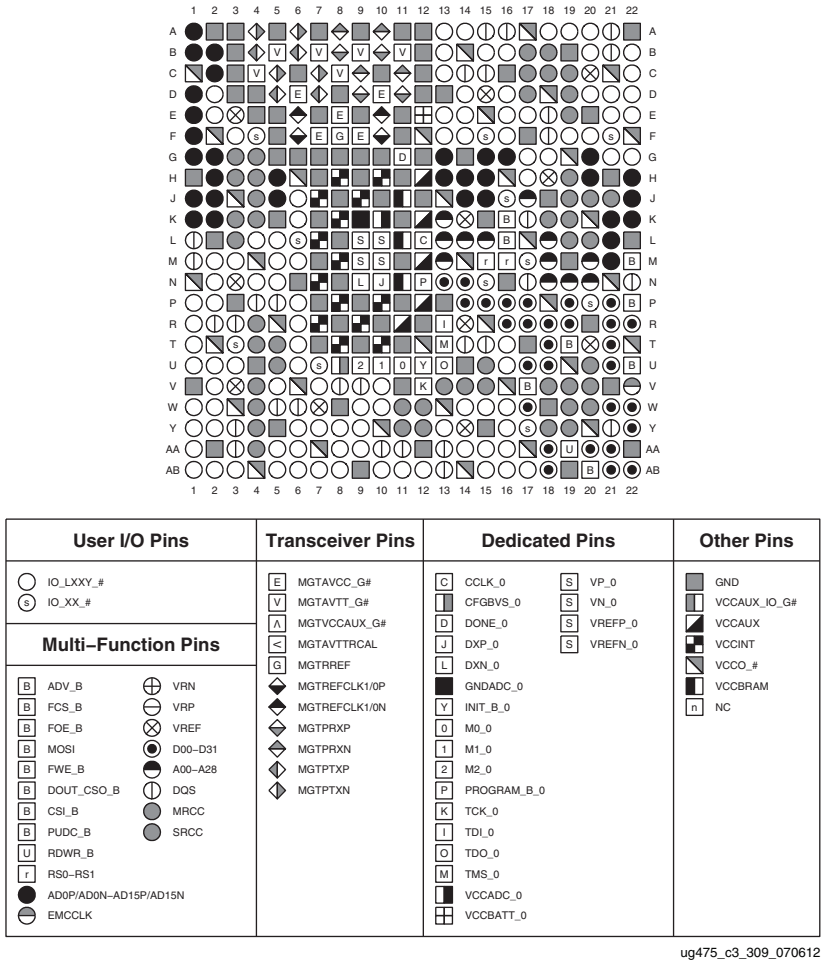

Figure 3-17: **SBG484 Package—XC7A200T Pinout Diagram**

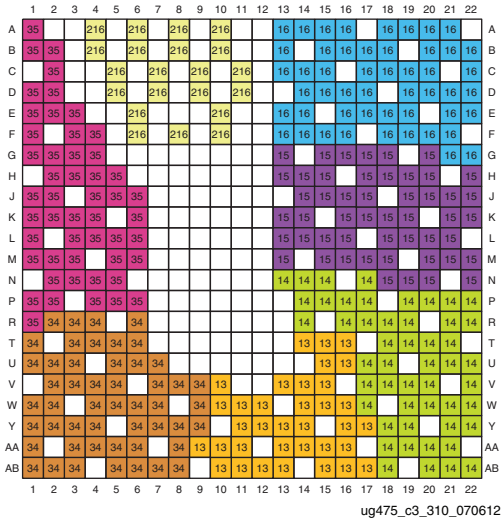

Figure 3-18: **SBG484 Package—XC7A200T I/O Banks**

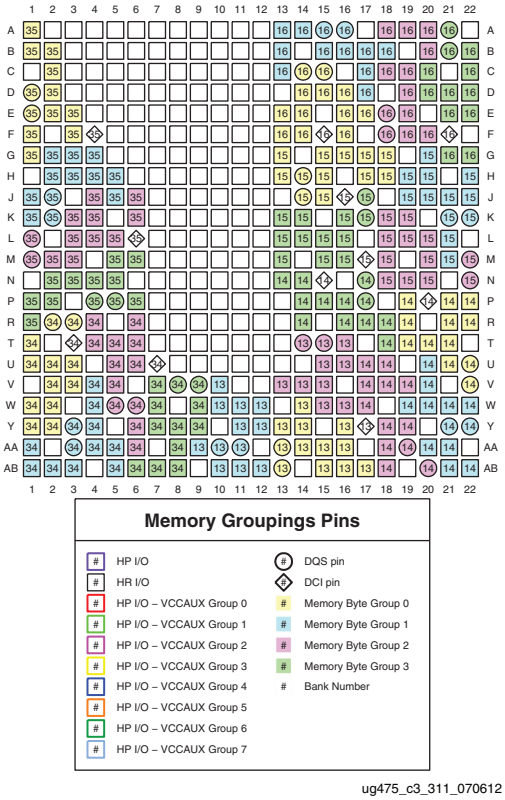

Figure 3-19: **SBG484 Package—XC7A200T Memory Groupings**

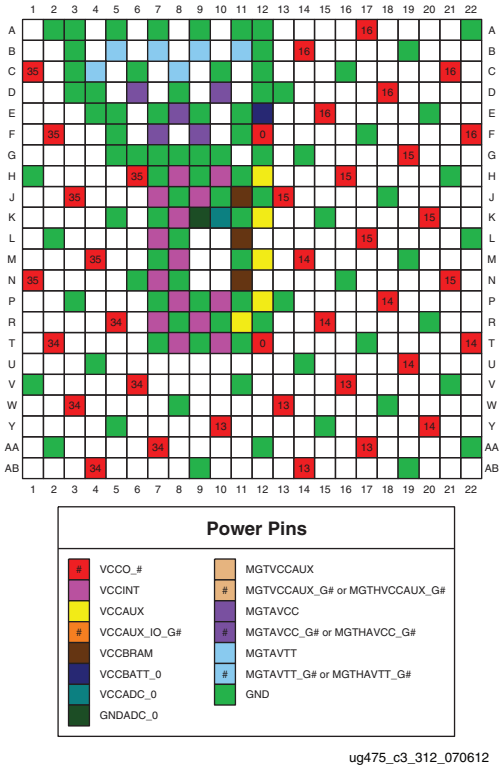

Figure 3-20: **SBG484 Package—XC7A200T Power and GND Placement**

FBG484 Package—XC7A200T

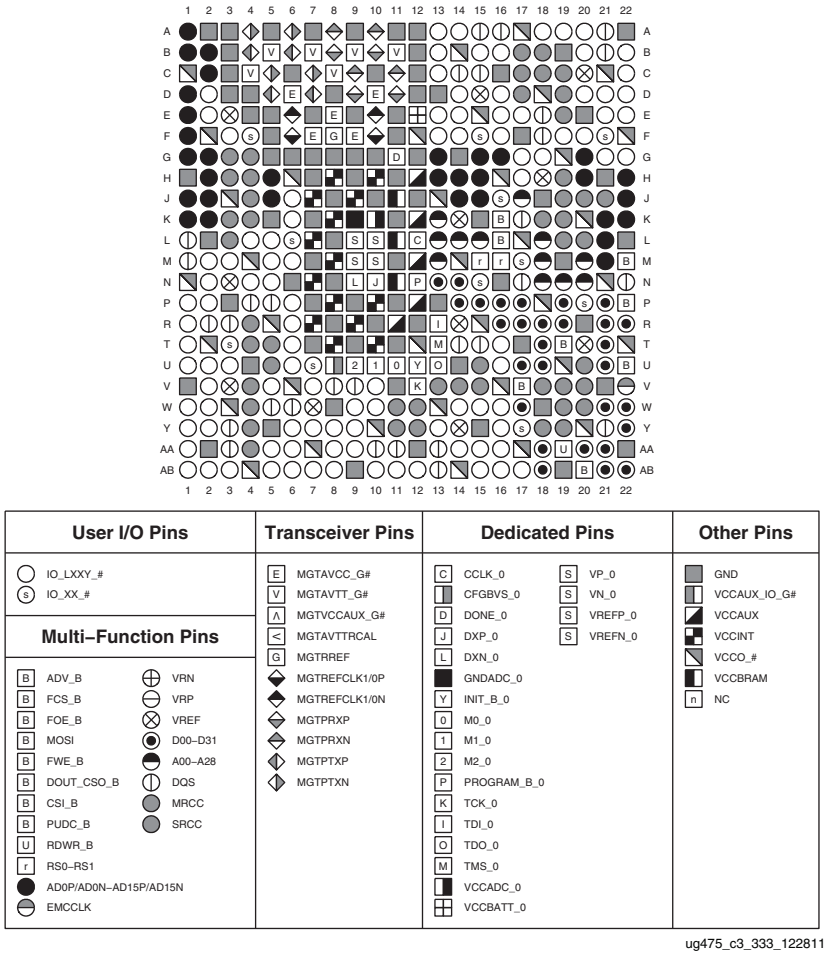

Figure 3-21: **FBG484 Package—XC7A200T Pinout Diagram**

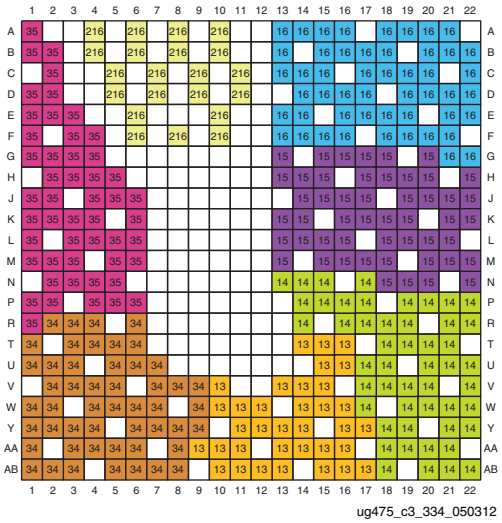

Figure 3-22: **FBG484 Package—XC7A200T I/O Banks**

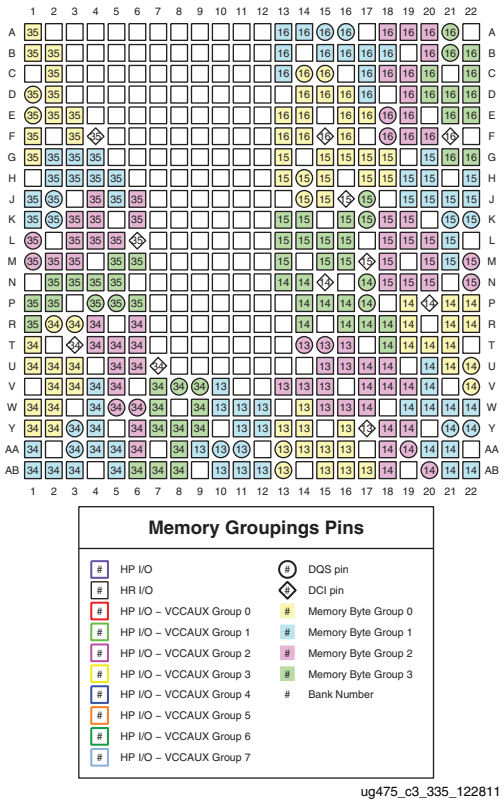

Figure 3-23: **FBG484 Package—XC7A200T Memory Groupings**

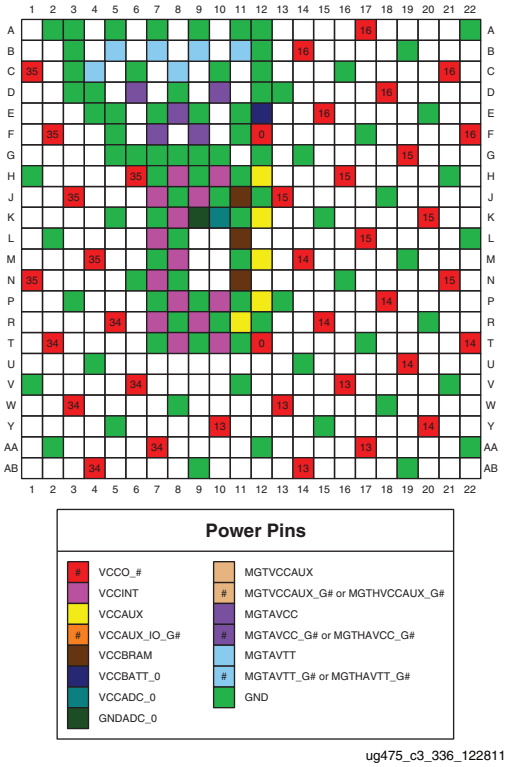

Figure 3-24: **FBG484 Package—XC7A200T Power and GND Placement**

FBG676 Package—XC7A200T

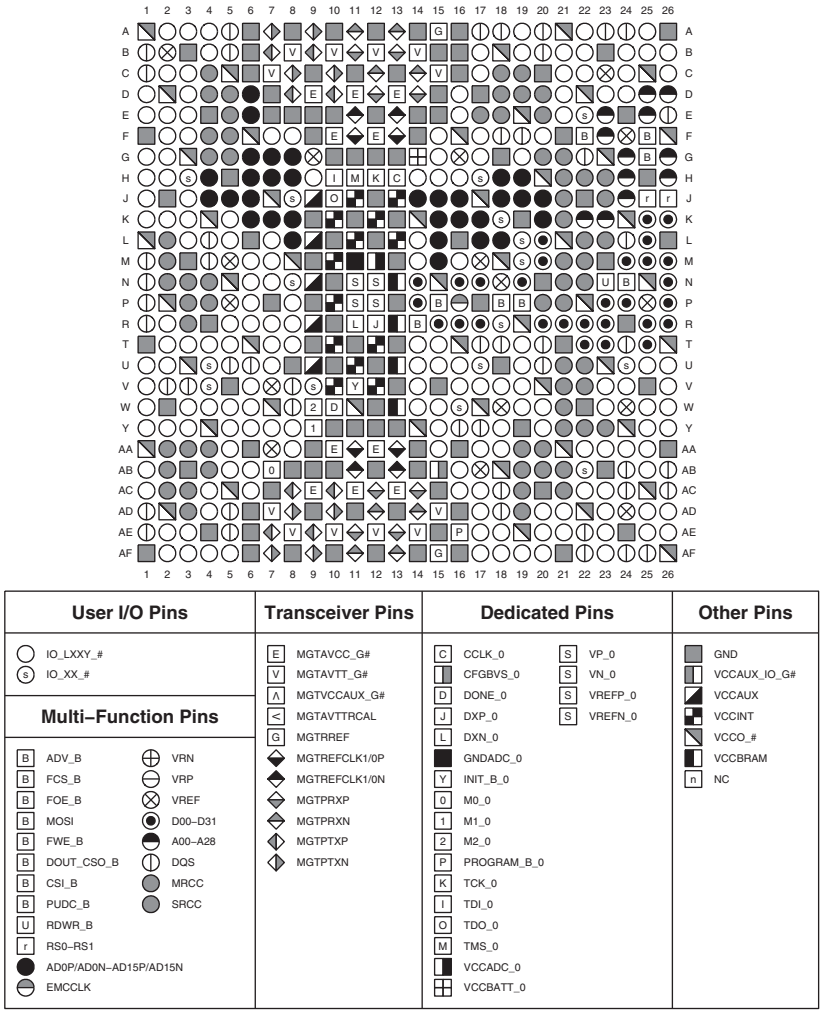

Figure 3-25: **FBG676 Package—XC7A200T Pinout Diagram**

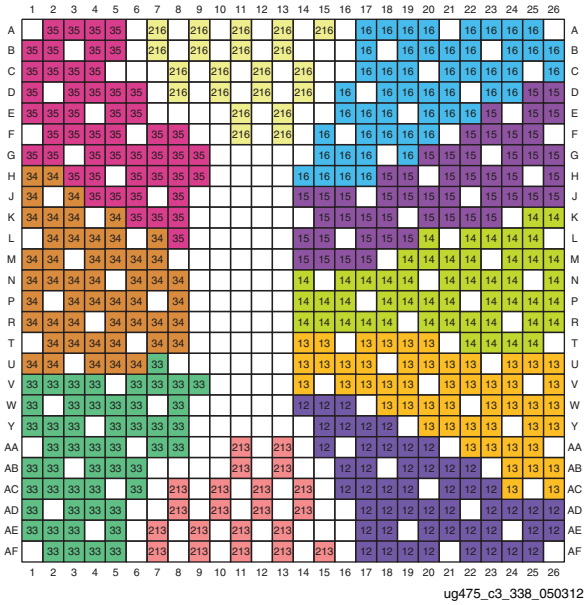

Figure 3-26: **FBG676 Package—XC7A200T I/O Banks**

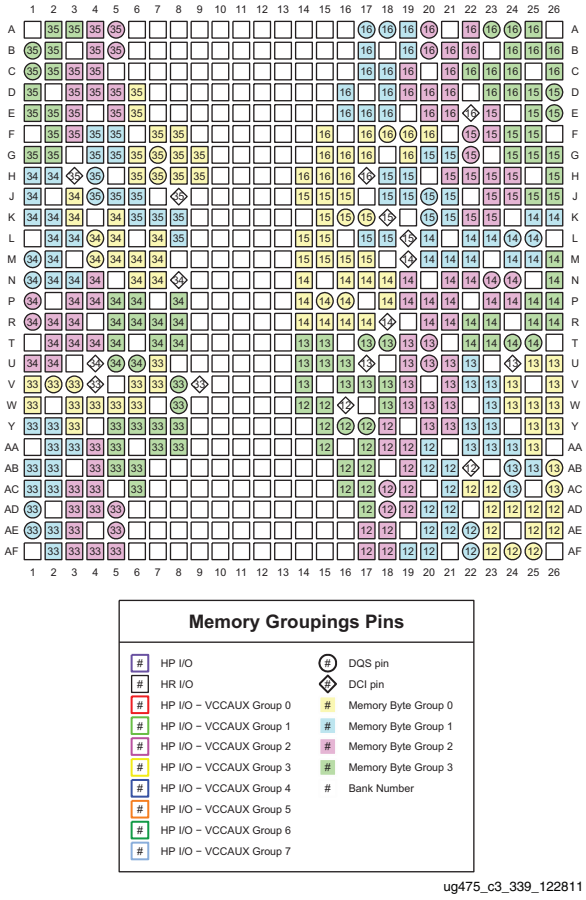

Figure 3-27: **FBG676 Package—XC7A200T Memory Groupings**

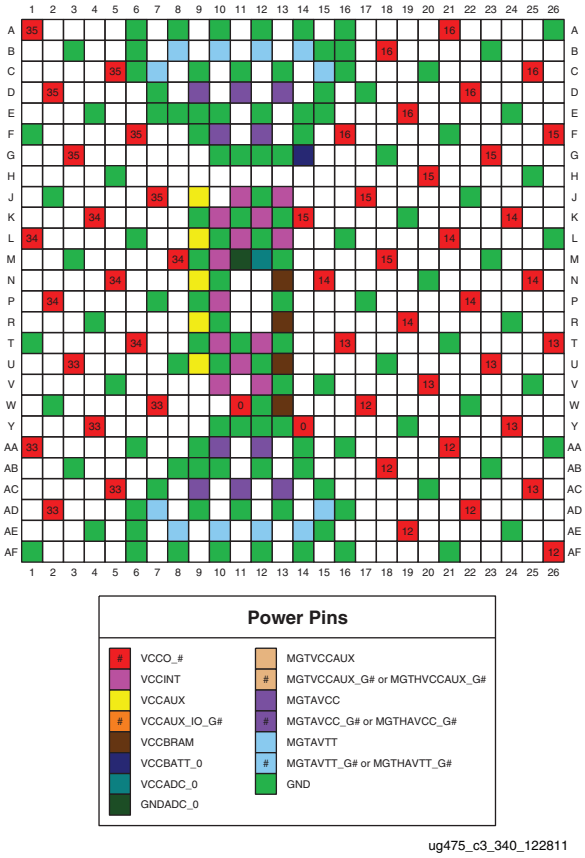

Figure 3-28: **FBG676 Package—XC7A200T Power and GND Placement**

FFG1156 Package—XC7A200T

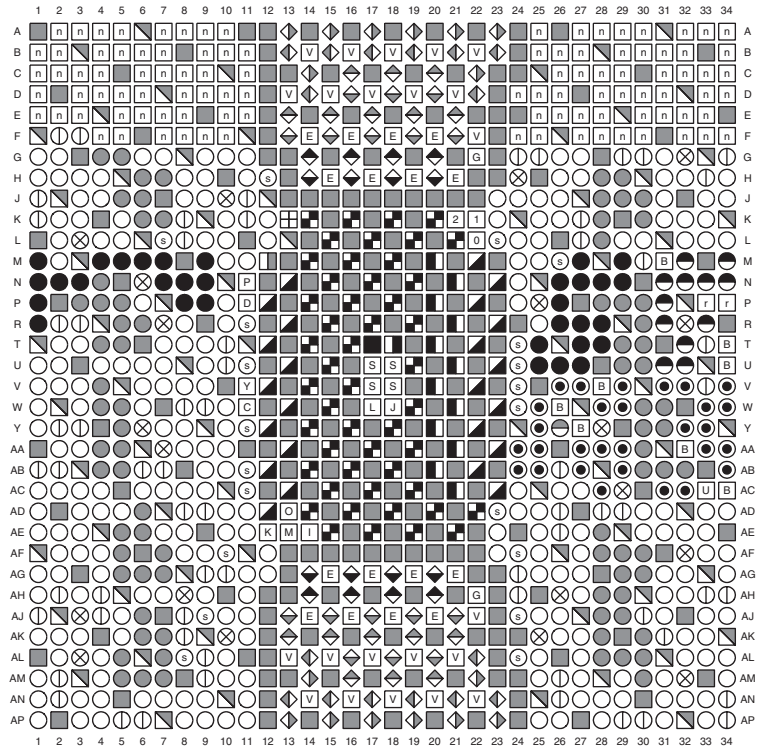

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Figure 3-29: **FFG1156 Package—XC7A200T Pinout Diagram**

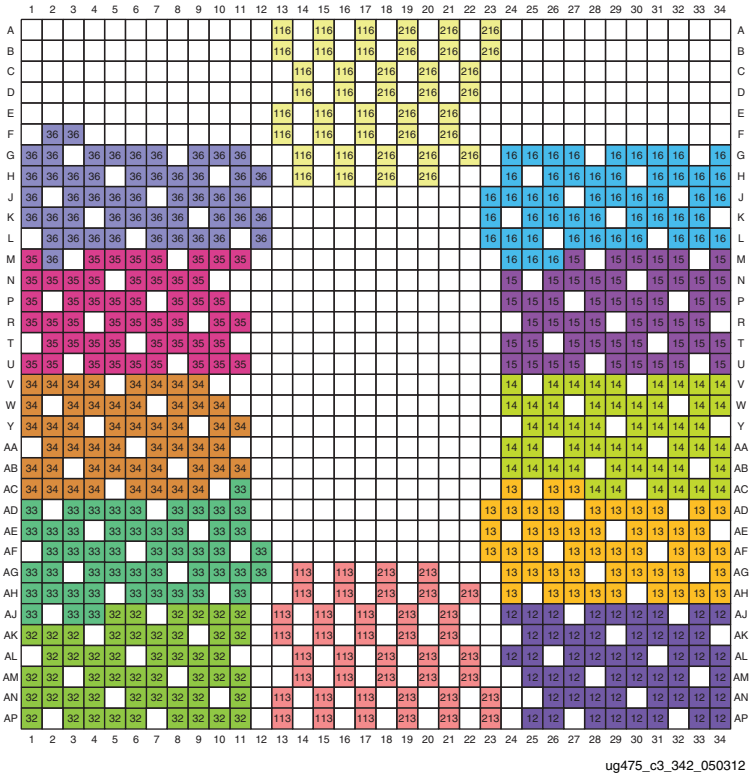


Figure 3-30: **FFG1156 Package—XC7A200T I/O Banks**

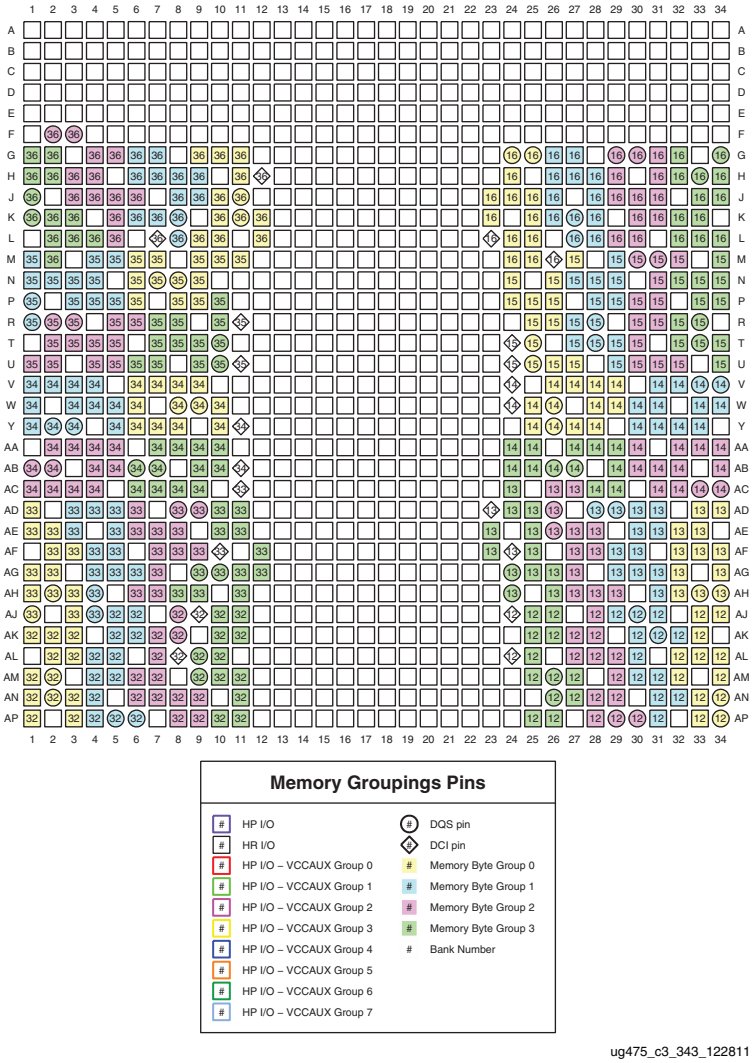


Figure 3-31: **FFG1156 Package—XC7A200T Memory Groupings**

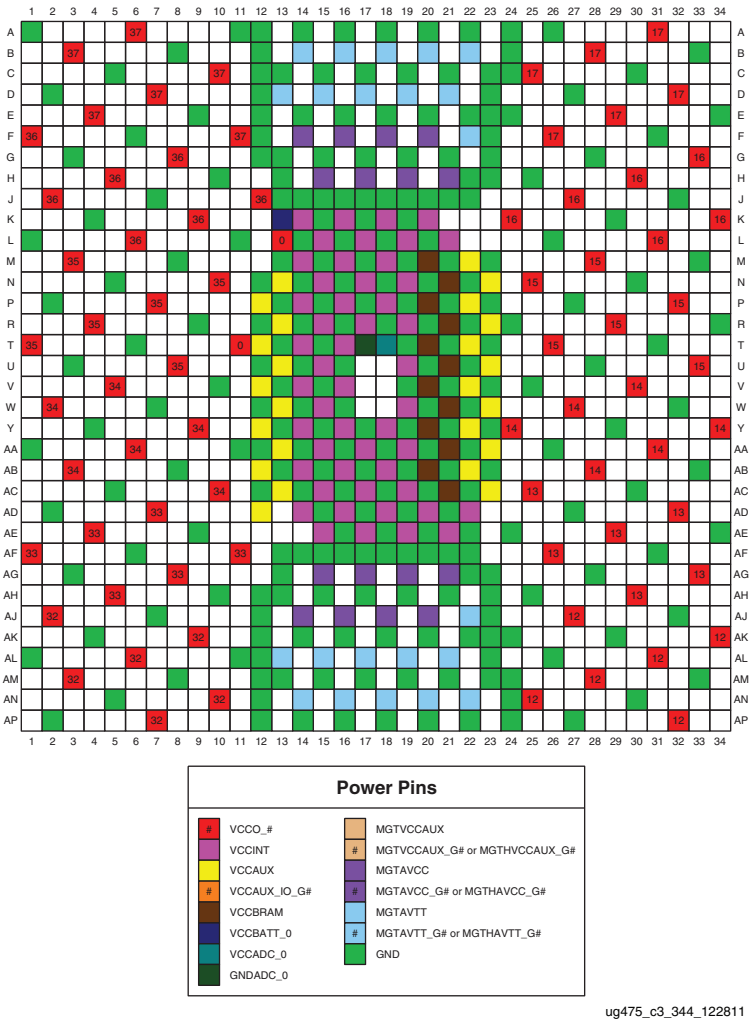


Figure 3-32: **FFG1156 Package—XC7A200T Power and GND Placement**

Kintex-7 FPGAs Device Diagrams

Table 3-2: **Kintex-7 FPGAs Device Diagrams Cross-Reference**

Device	FB/FBG484	FB/FBG676	FB/FBG900	FF/FFG676	FF/FFG900	FF/FFG901	FF/FFG1156
XC7K70T	page 81	page 84					
XC7K160T	page 81	page 87		page 94			
XC7K325T		page 87	page 90	page 94	page 97		
XC7K355T						page 101	
XC7K410T		page 87	page 90	page 94	page 97		
XC7K420T						page 105	page 109
XC7K480T						page 105	page 109

FBG484 Package—XC7K70T and XC7K160T

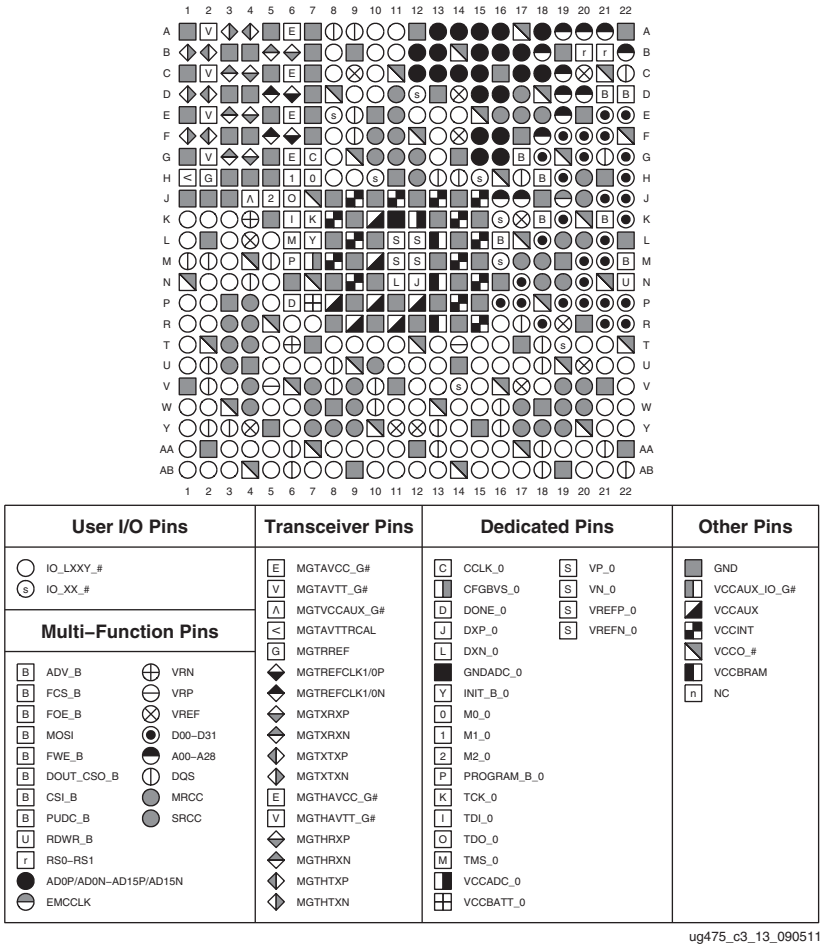


Figure 3-33: **FBG484 Package—XC7K70T and XC7K160T Pinout Diagram**

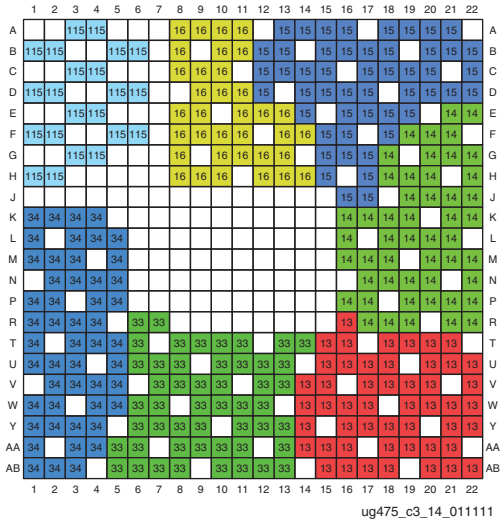


Figure 3-34: **FBG484 Package—XC7K70T and XC7K160T I/O Banks**

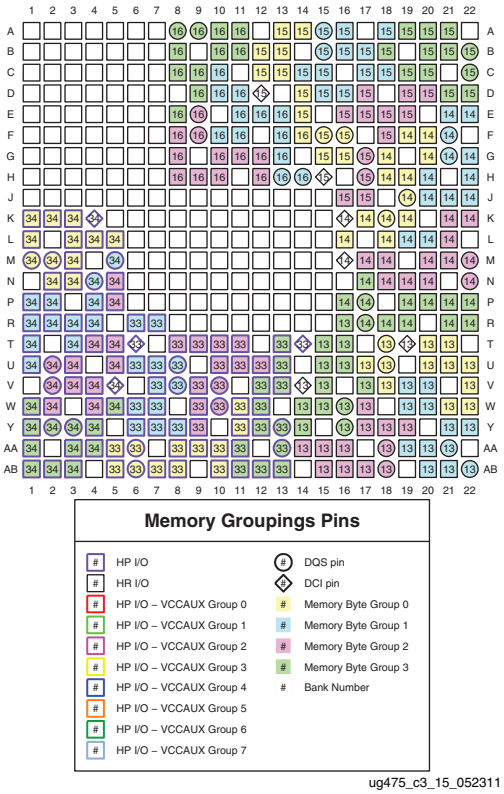


Figure 3-35: **FBG484 Package—XC7K70T and XC7K160T Memory Groupings**

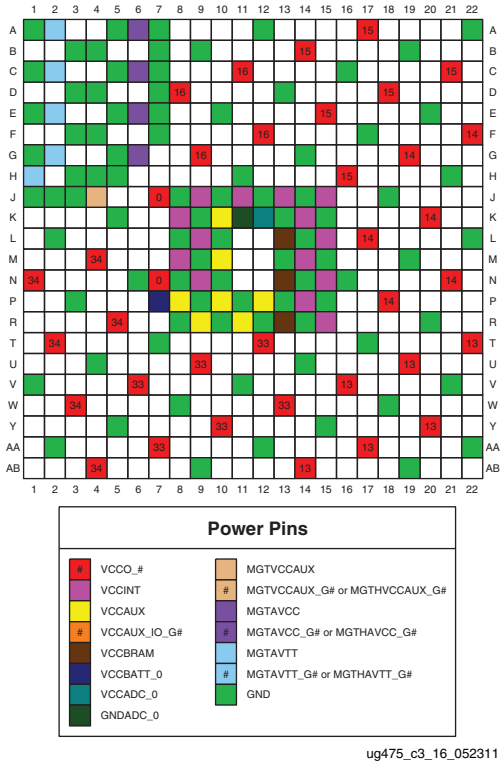
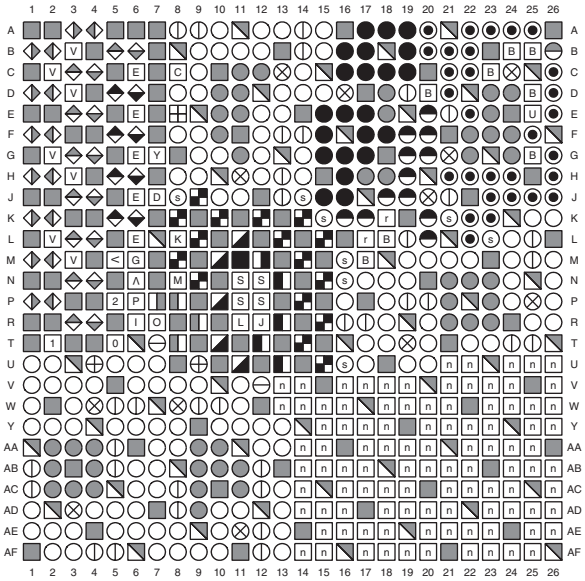


Figure 3-36: **FBG484 Package—XC7K70T and XC7K160T Power and GND Placement**

FBG676 Package—XC7K70T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	DONE_0	VCCAUX
ADV_B	MGTAVTTRCAL	DXP_0	VCCINT
FCS_B	MGTRREF	DXN_0	VCCO_#
FOE_B	MGTREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	MGTREFCLK1/0N	INIT_B_0	NC
FWE_B	MGTXRXP	M0_0	
DOUT_CSO_B	MGTXRXN	M1_0	
CSI_B	MGTXTXP	M2_0	
PUDC_B	MGTXTXN	PROGRAM_B_0	
RDWR_B	MGTHAVCC_G#	TCK_0	
RS0–RS1	MGTHAVTT_G#	TDI_0	
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0	
EMCCLK	MGTHRXN	TMS_0	
VRN	MGTHTXP	VCCADC_0	
VRP	MGTHTXN	VCCBATT_0	
VREF		VP_0	
D00–D31		VN_0	
A00–A28		VREFP_0	
DQS		VREFN_0	
MRCC			
SRCC			

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Figure 3-37: **FBG676 Package—XC7K70T Pinout Diagram**

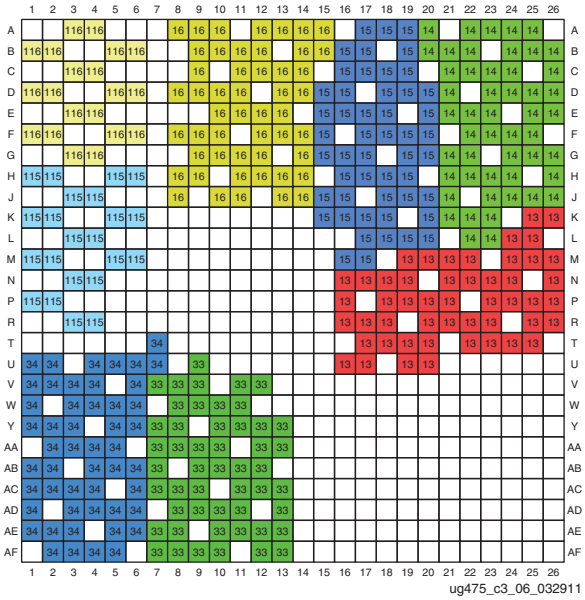


Figure 3-38: **FBG676 Package—XC7K70T I/O Banks**

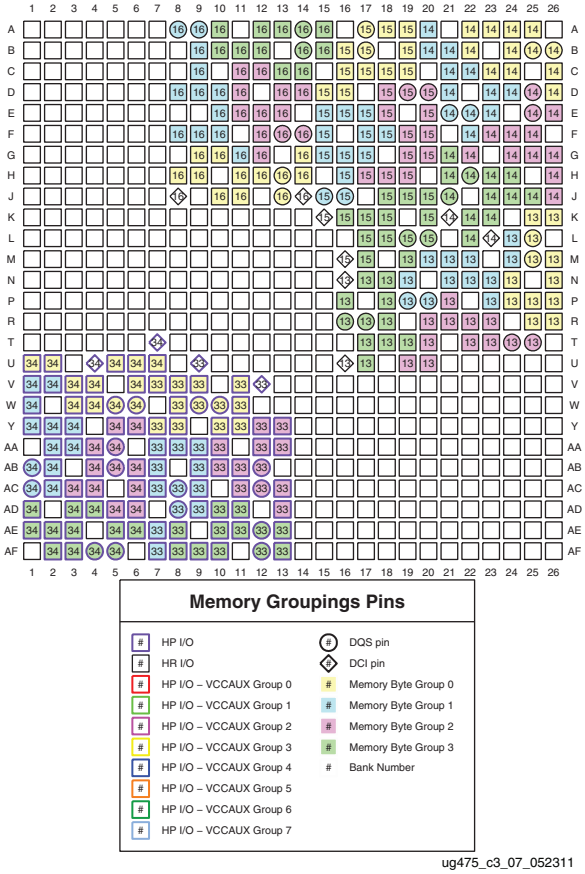


Figure 3-39: **FBG676 Package—XC7K70T Memory Groupings**

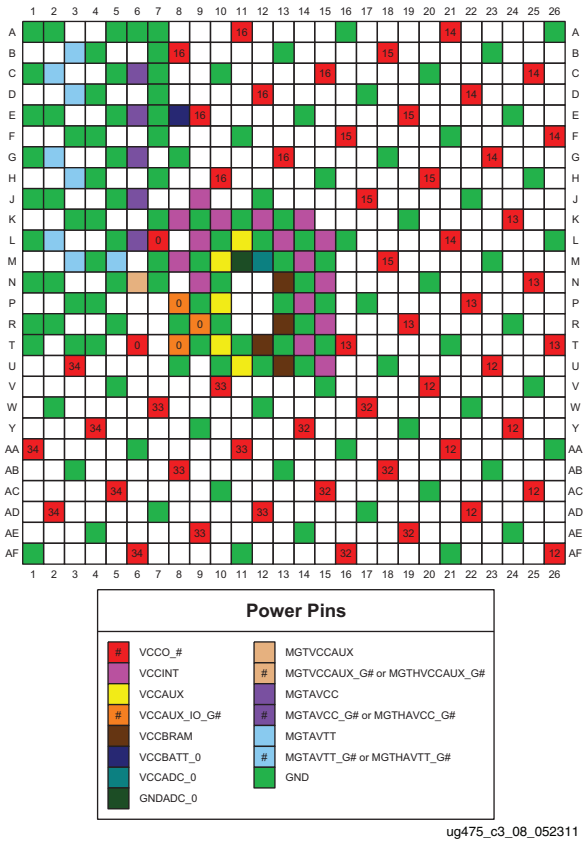
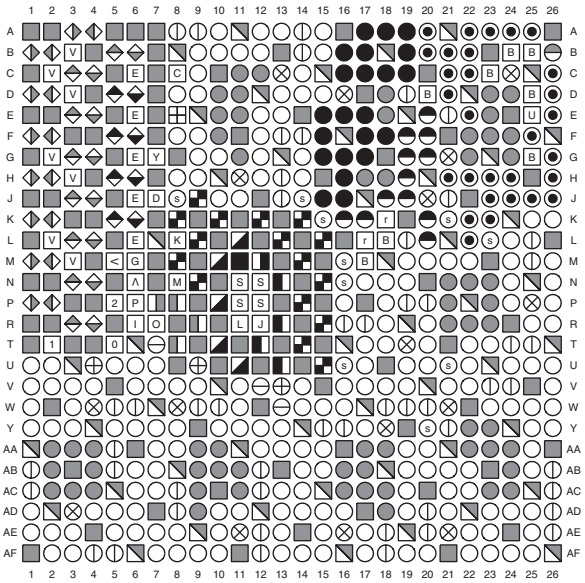


Figure 3-40: **FBG676 Package—XC7K70T Power and GND Placement**

FBG676 Package—XC7K160T, XC7K325T, and XC7K410T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	DONE_0	VCCAUX
ADV_B	MGTAVTTRCAL	DXP_0	VCCINT
FCS_B	MGTRREF	DXN_0	VCCO_#
FOE_B	MGTREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	MGTREFCLK1/0N	INIT_B_0	NC
FWE_B	MGTXRXP	M0_0	
DOUT_CSO_B	MGTXRXN	M1_0	
CSI_B	MGTXTXP	M2_0	
PUDC_B	MGTXTXN	PROGRAM_B_0	
RDWR_B	MGTHAVCC_G#	TCK_0	
RS0–RS1	MGTHAVTT_G#	TDI_0	
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0	
EMCCLK	MGTHRXN	TMS_0	
VRN	MGTHTXP	VCCADC_0	
VRP	MGTHTXN	VCCBATT_0	
VREF		VP_0	
D00–D31		VN_0	
A00–A28		VREFP_0	
DQS		VREFN_0	
MRCC			
SRCC			

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Figure 3-41: **FBG676 Package—XC7K160T, XC7K325T, and XC7K410T Pinout Diagram**

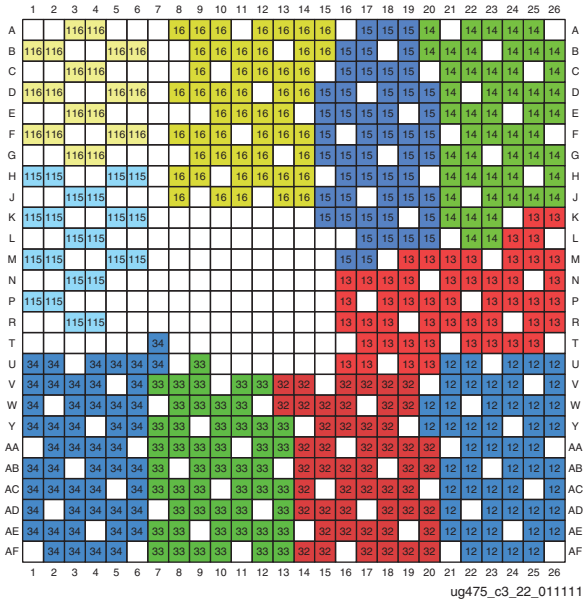


Figure 3-42: **FBG676 Package—XC7K160T, XC7K325T, and XC7K410T I/O Banks**

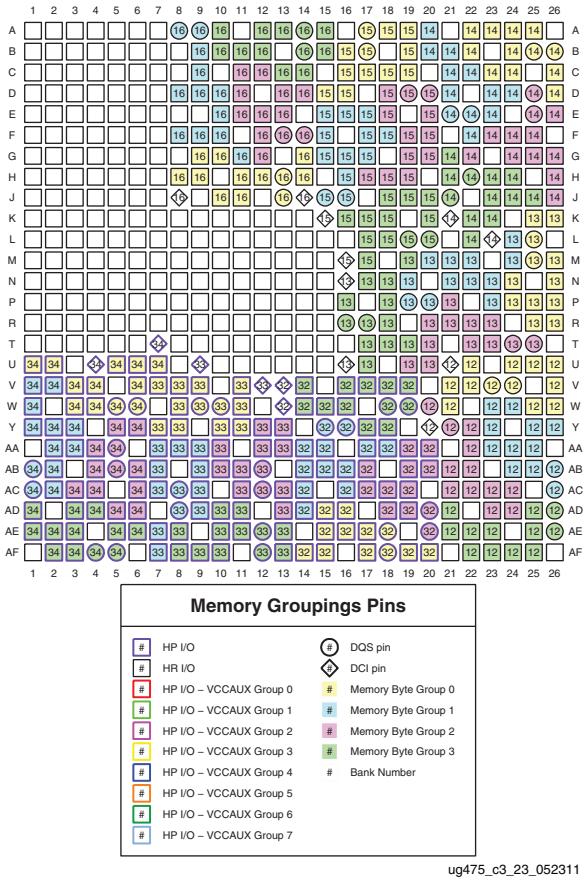


Figure 3-43: **FBG676 Package—XC7K160T, XC7K325T, and XC7K410T Memory Groupings**

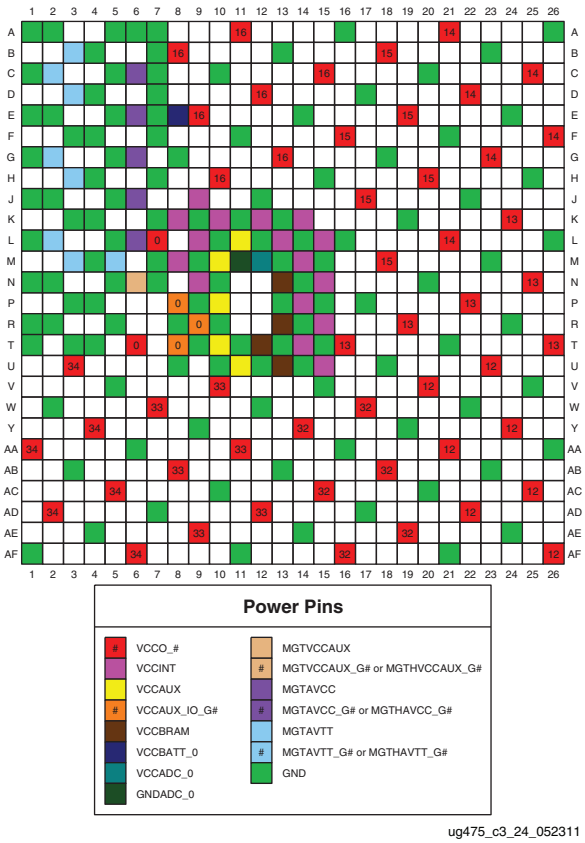
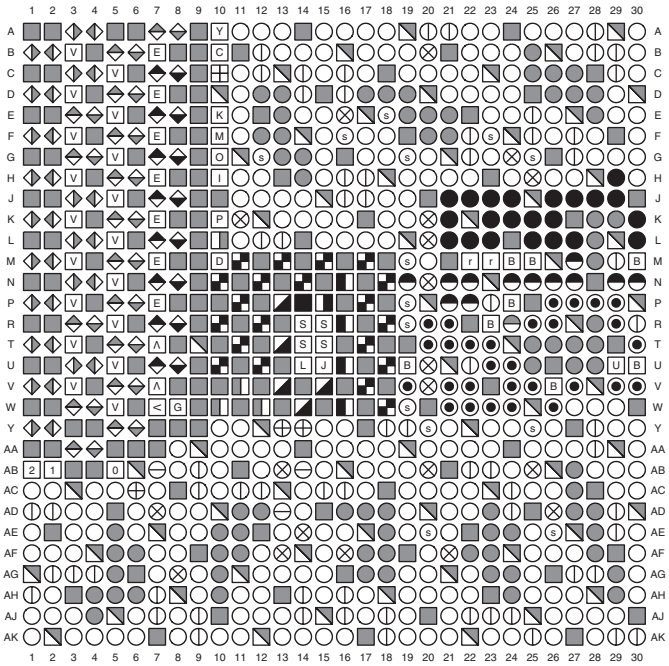


Figure 3-44: **FBG676 Package—XC7K160T, XC7K325T, and XC7K410T Power and GND Placement**

FBG900 Package—XC7K325T and XC7K410T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	DONE_0	VCCAUX
ADV_B	MGTAVTTRCAL	DXP_0	VCCINT
FCS_B	MGTRREF	DXN_0	VCCO_#
FOE_B	MGTREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	MGTREFCLK1/0N	INIT_B_0	NC
FWE_B	MGTXRXP	M0_0	
DOUT_CSO_B	MGTXRXN	M1_0	
CSI_B	MGTXTXP	M2_0	
PUDC_B	MGTXTXN	PROGRAM_B_0	
RDWR_B	MGTHAVCC_G#	TCK_0	
RS0–RS1	MGTHAVTT_G#	TDI_0	
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0	
EMCCLK	MGTHRXN	TMS_0	
VRN	MGTHTXP	VCCADC_0	
VRP	MGTHTXN	VCCBATT_0	
VREF		VP_0	
D00–D31		VN_0	
A00–A28		VREFP_0	
DQS		VREFN_0	
MRCC			
SRCC			

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Figure 3-45: **FBG900 Package—XC7K325T and XC7K410T Pinout Diagram**

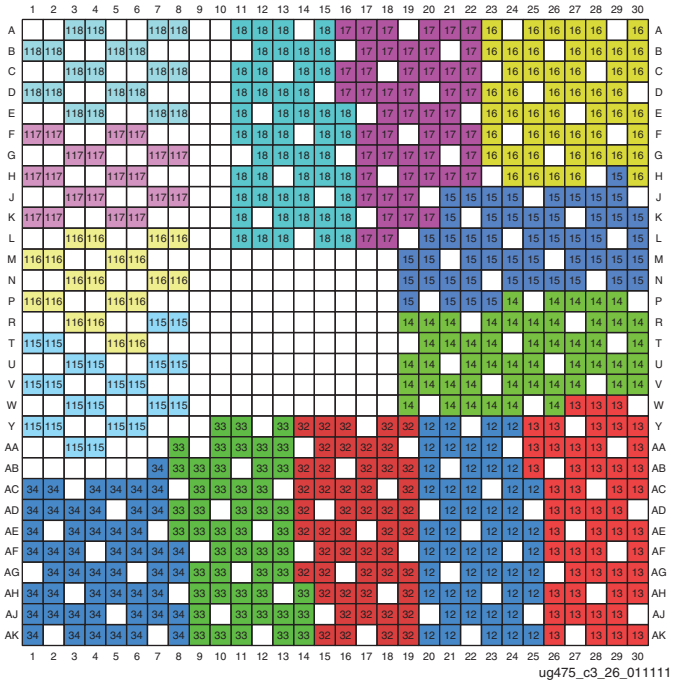


Figure 3-46: **FBG900 Package—XC7K325T and XC7K410T I/O Banks**

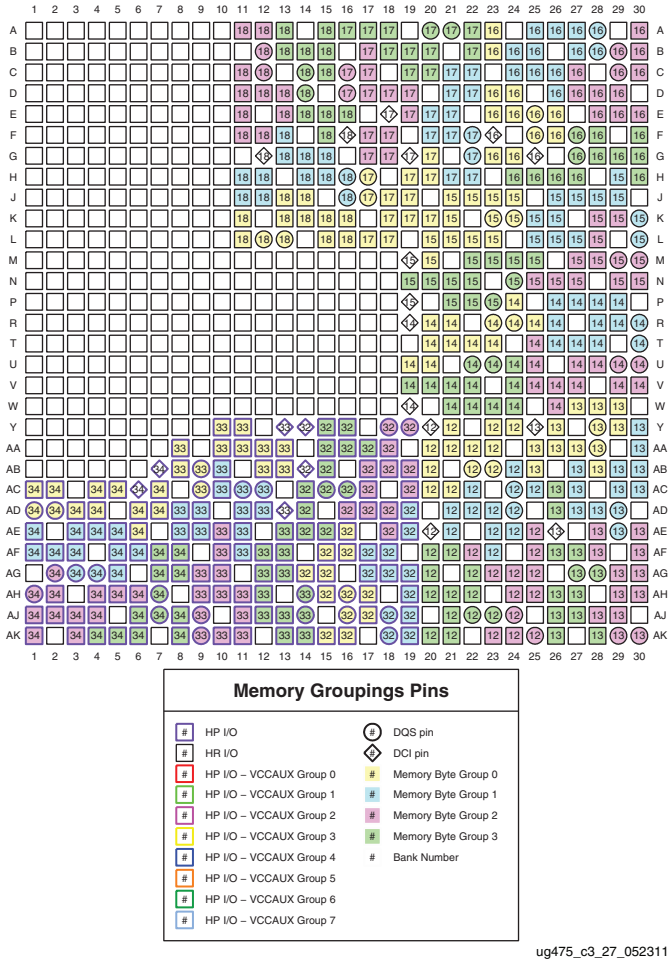


Figure 3-47: **FBG900 Package—XC7K325T and XC7K410T Memory Groupings**

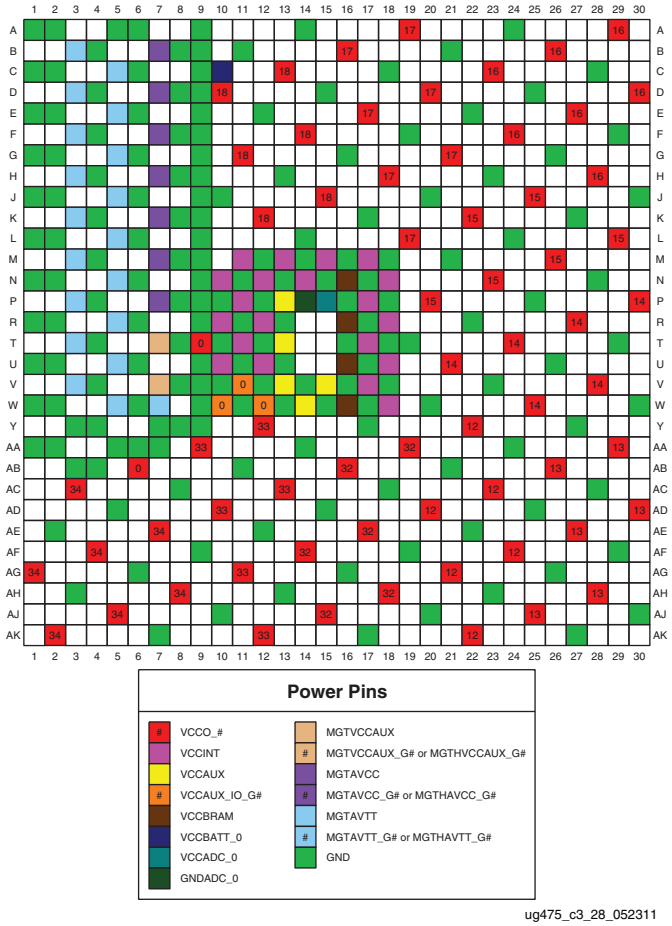


Figure 3-48: **FBG900 Package—XC7K325T and XC7K410T Power and GND Placement**

FFG676 Package—XC7K160T, XC7K325T, and XC7K410T

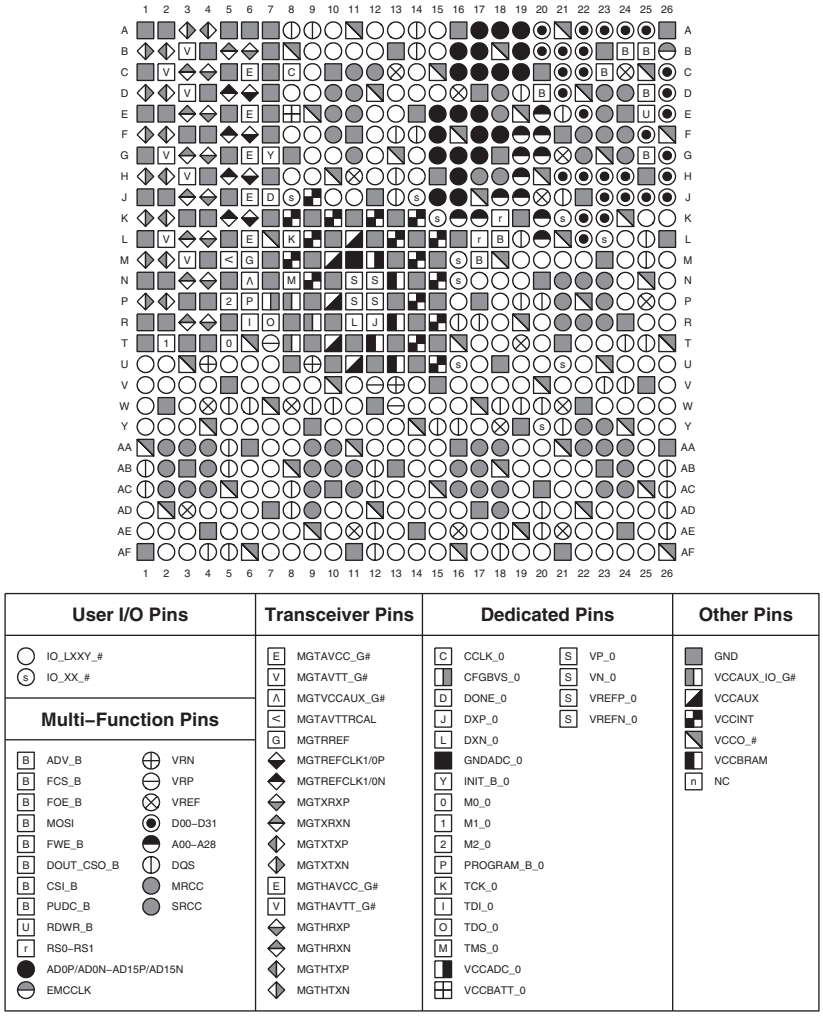


Figure 3-49: **FFG676 Package—XC7K160T, XC7K325T, and XC7K410T Pinout Diagram**

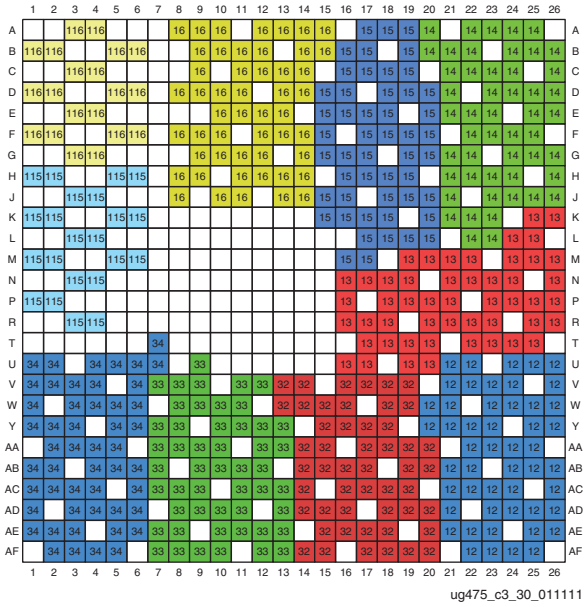


Figure 3-50: **FFG676 Package—XC7K160T, XC7K325T, and XC7K410T I/O Banks**

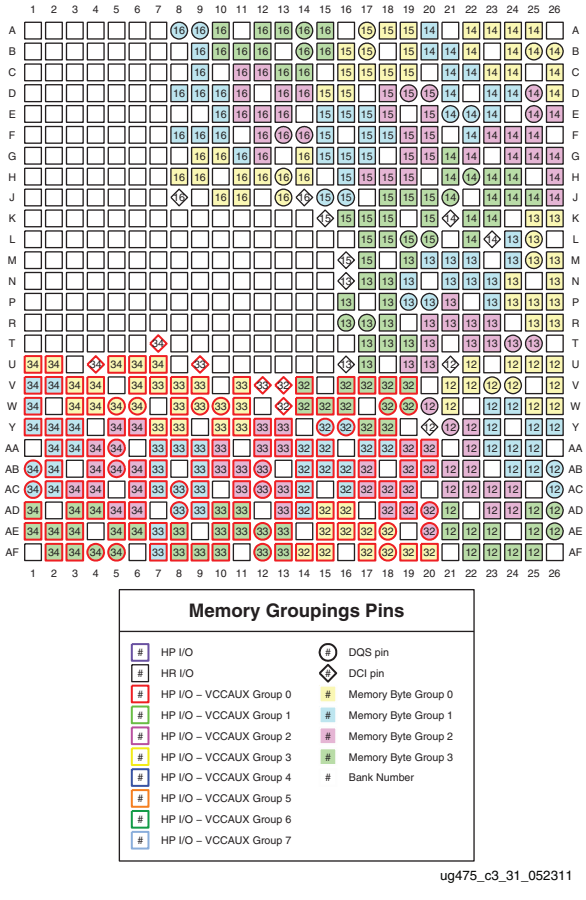


Figure 3-51: **FFG676 Package—XC7K160T, XC7K325T, and XC7K410T Memory Groupings**

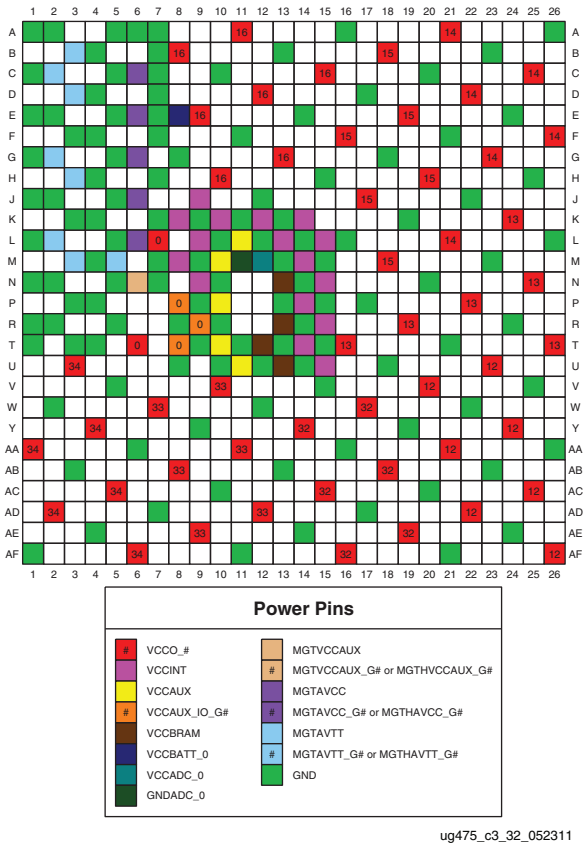
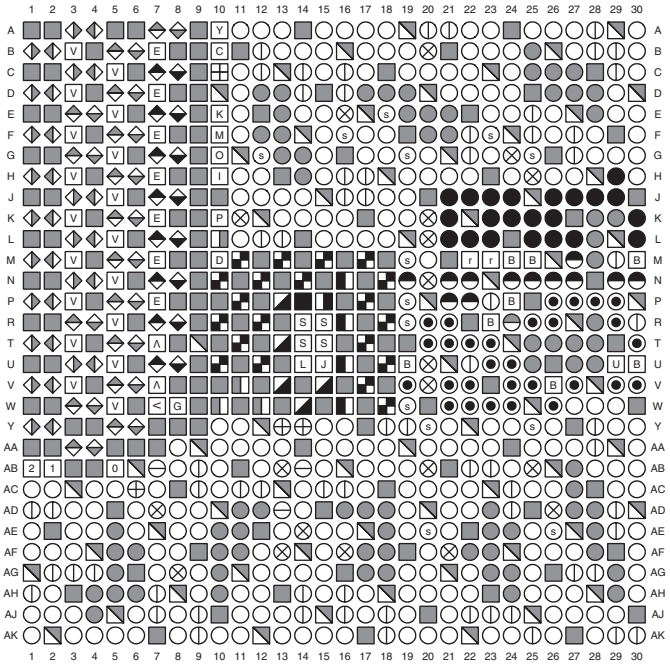


Figure 3-52: **FFG676 Package—XC7K160T, XC7K325T, and XC7K410T Power and GND Placement**

FFG900 Package—XC7K325T and XC7K410T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	DONE_0	VCCAUX
ADV_B	MGTAVTTRCAL	DXP_0	VCCINT
FCS_B	MGTRREF	DXN_0	VCCO_#
FOE_B	MGTREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	MGTREFCLK1/0N	INIT_B_0	NC
FWE_B	MGTXRXP	M0_0	
DOUT_CSO_B	MGTXRXN	M1_0	
CSI_B	MGTXTXP	M2_0	
PUDC_B	MGTXTXN	PROGRAM_B_0	
RDWR_B	MGTHAVCC_G#	TCK_0	
RS0–RS1	MGTHAVTT_G#	TDI_0	
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0	
EMCCLK	MGTHRXN	TMS_0	
VRN	MGTHTXP	VCCADC_0	
VRP	MGTHTXN	VCCBATT_0	
VREF		VP_0	
D00–D31		VN_0	
A00–A28		VREFP_0	
DQS		VREFN_0	
MRCC			
SRCC			

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Figure 3-53: **FFG900 Package—XC7K325T and XC7K410T Pinout Diagram**

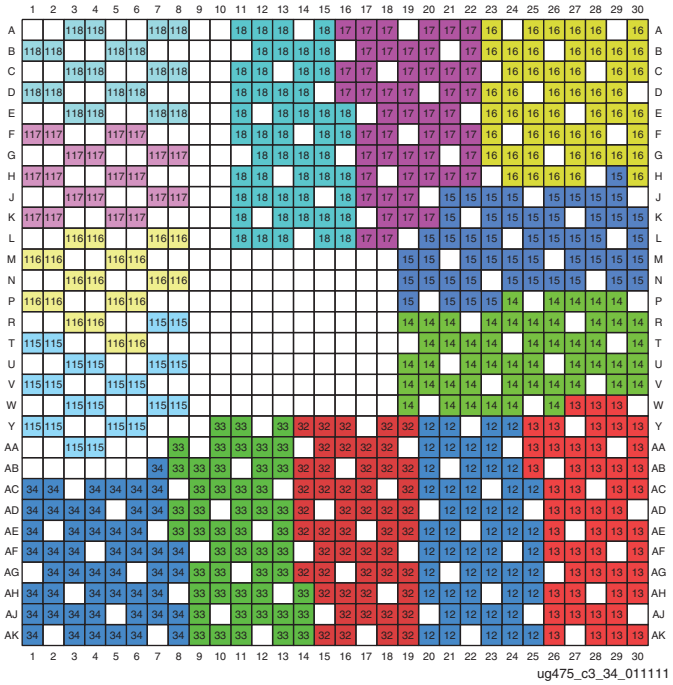


Figure 3-54: **FFG900 Package—XC7K325T and XC7K410T I/O Banks**

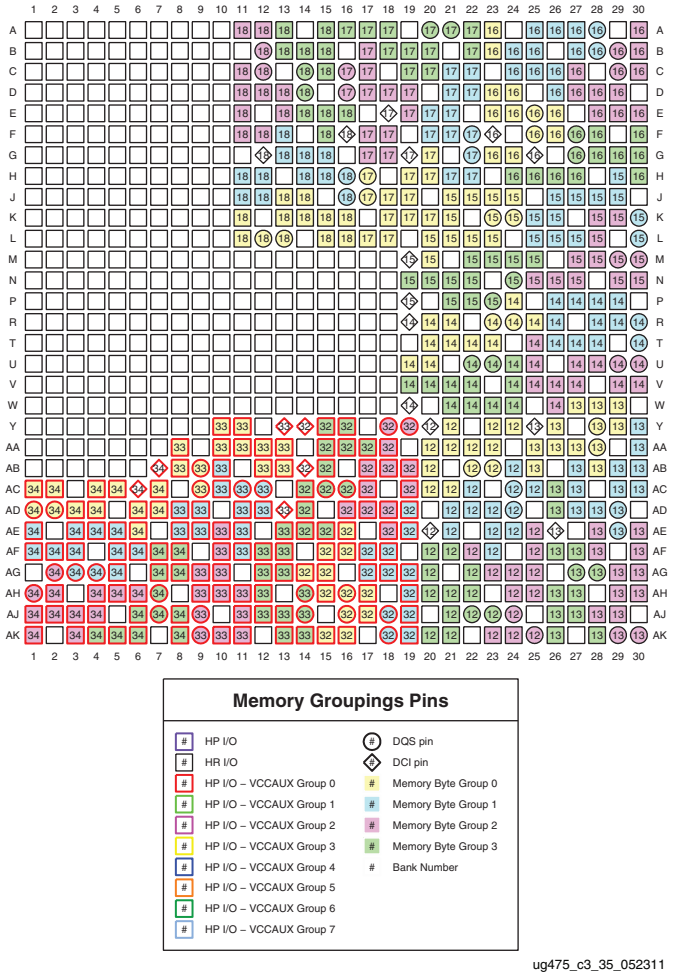


Figure 3-55: **FFG900 Package—XC7K325T and XC7K410T Memory Groupings**

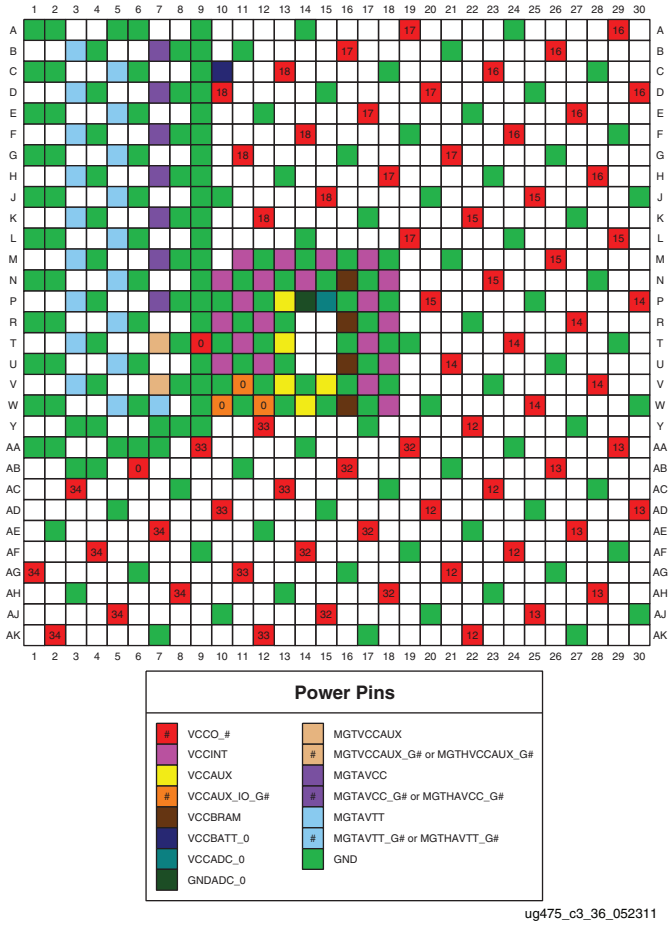


Figure 3-56: **FFG900 Package—XC7K325T and XC7K410T Power and GND Placement**

FFG901 Package—XC7K355T

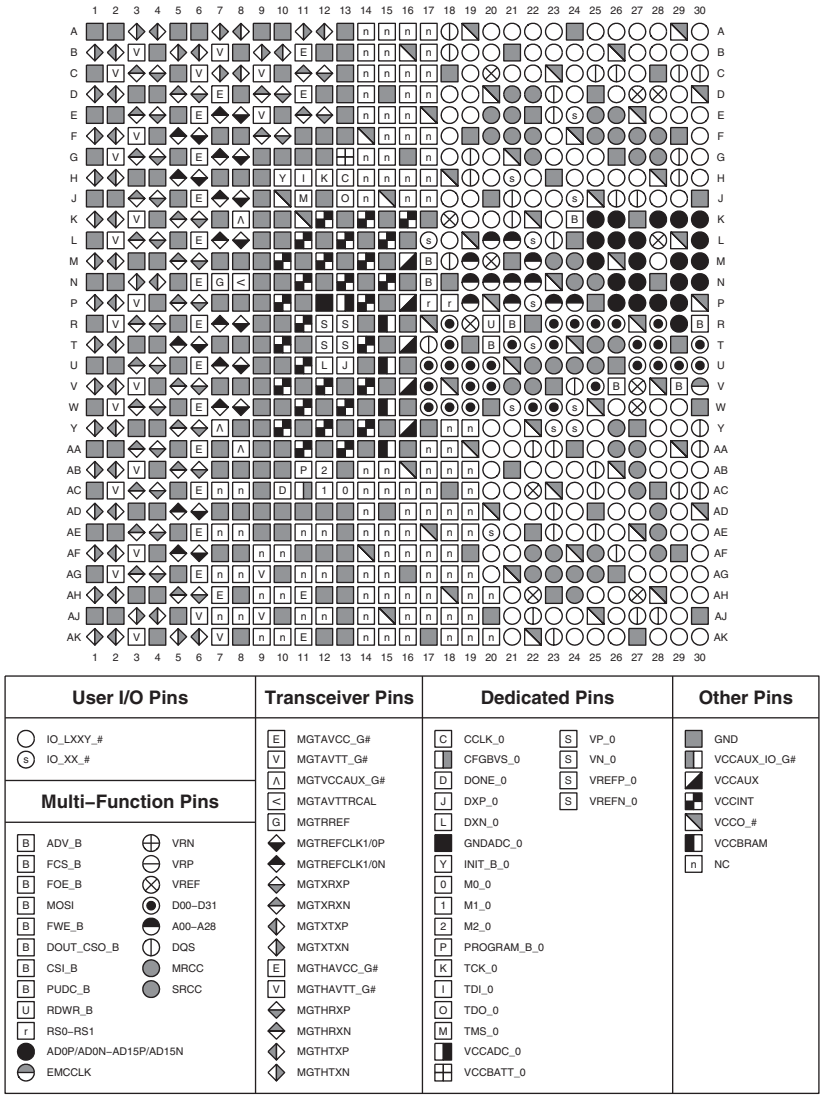


Figure 3-57: **FFG901 Package—XC7K355T Pinout Diagram**

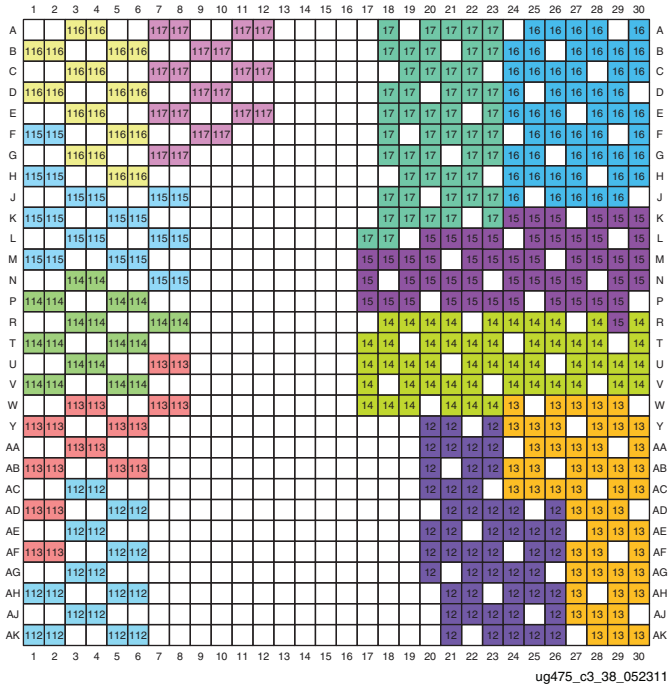


Figure 3-58: **FFG901 Package—XC7K355T I/O Banks**

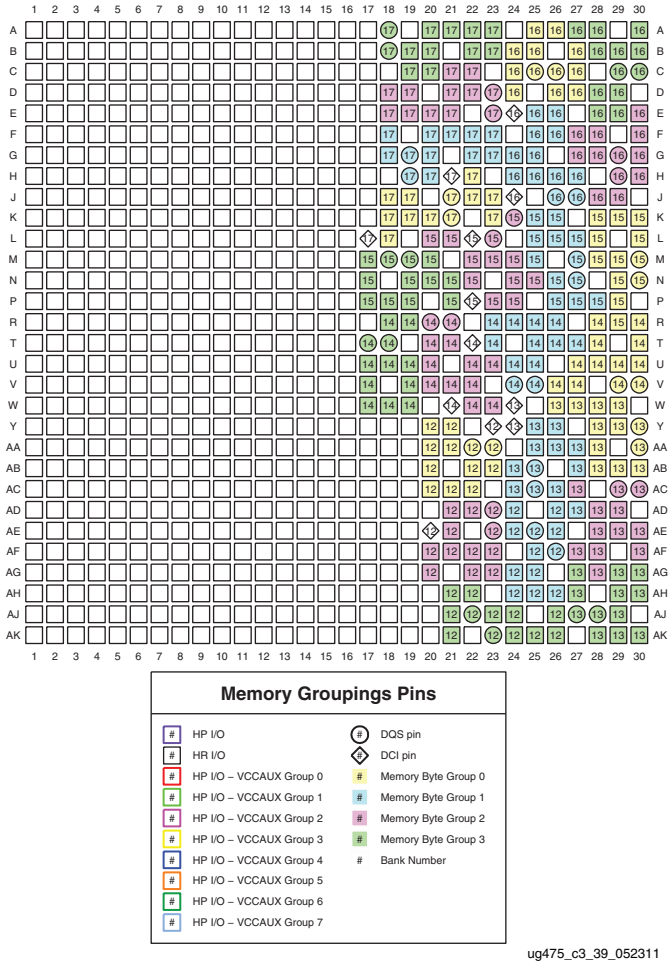


Figure 3-59: **FFG901 Package—XC7K355T Memory Groupings**

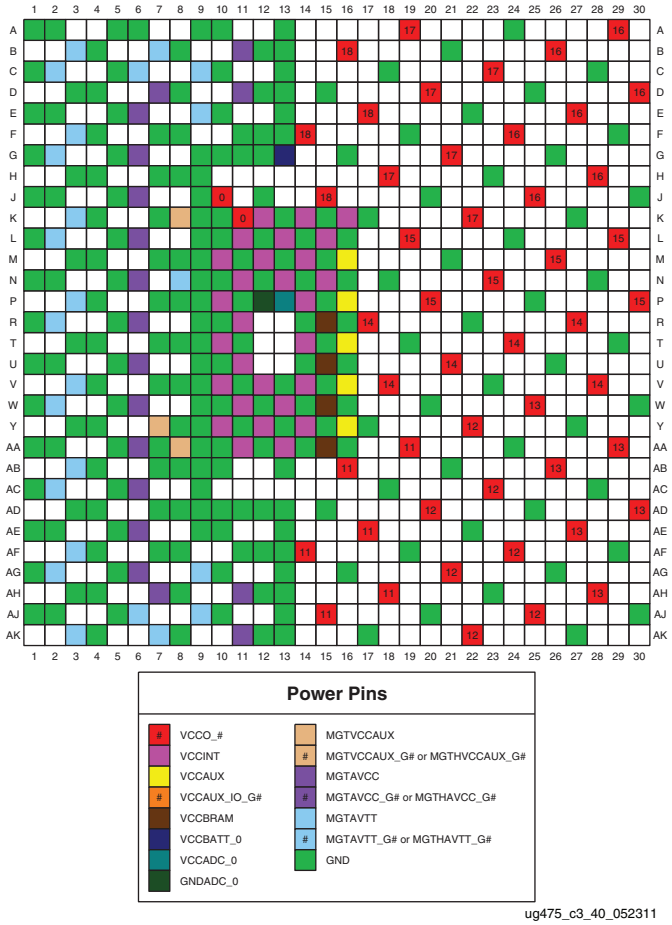


Figure 3-60: **FFG901 Package—XC7K355T Power and GND Placement**

FFG901 Package—XC7K420T and XC7K480T

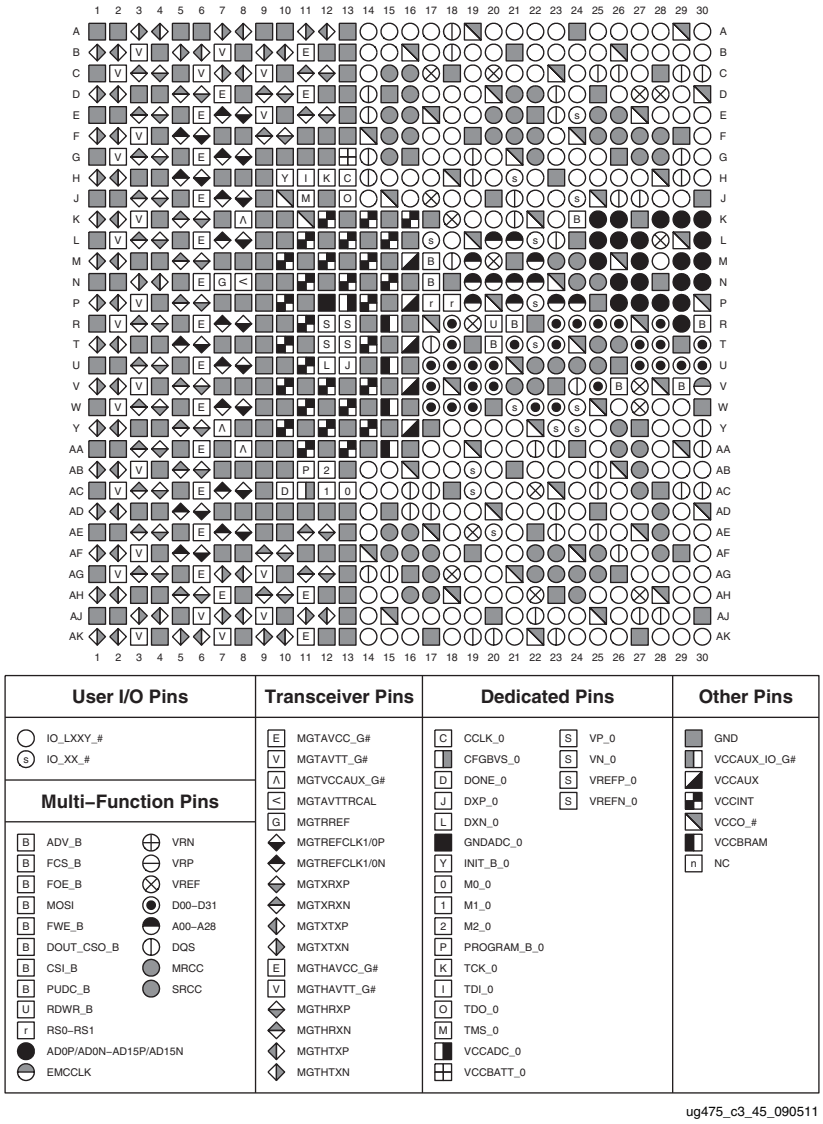


Figure 3-61: **FFG901 Package—XC7K420T and XC7K480T Pinout Diagram**

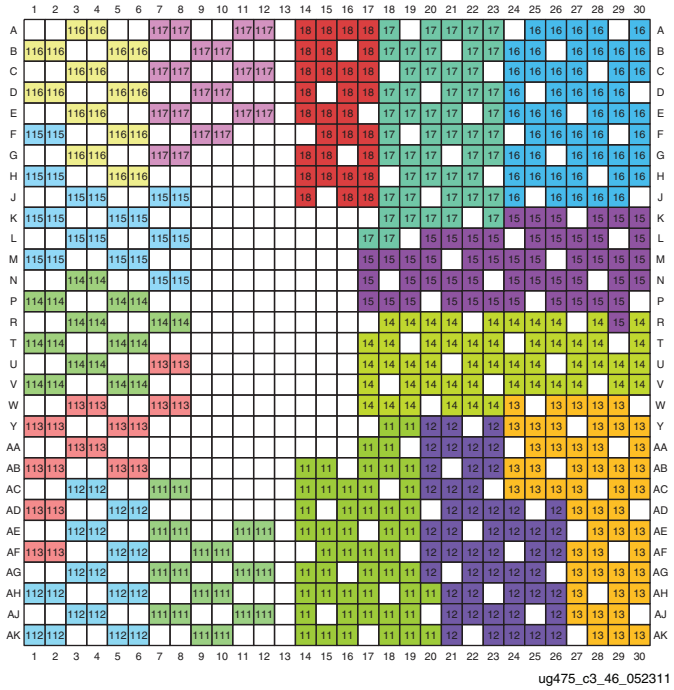


Figure 3-62: **FFG901 Package—XC7K420T and XC7K480T I/O Banks**

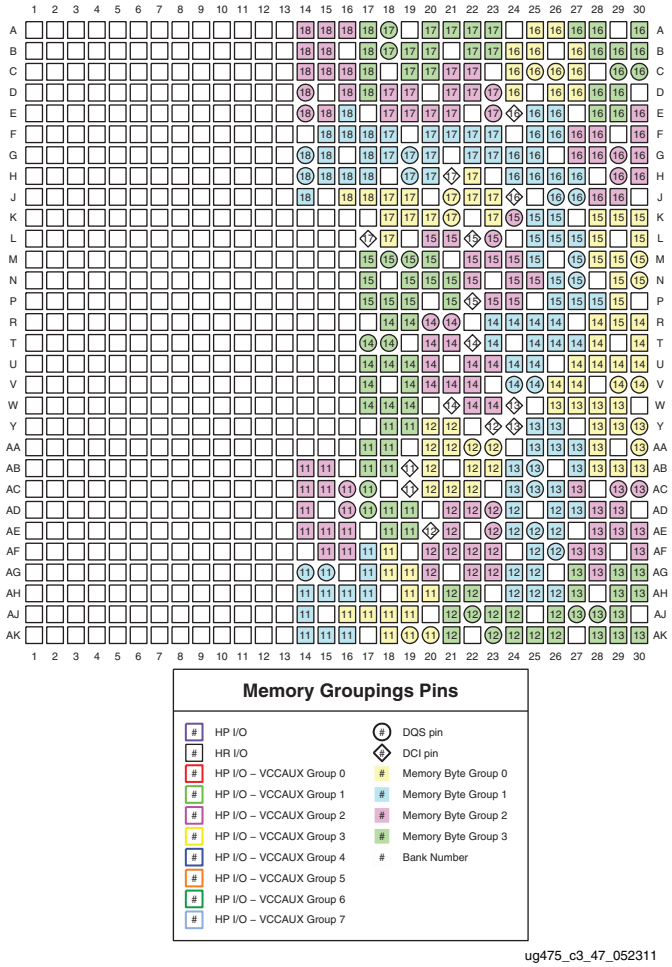


Figure 3-63: **FFG901 Package—XC7K420T and XC7K480T Memory Groupings**

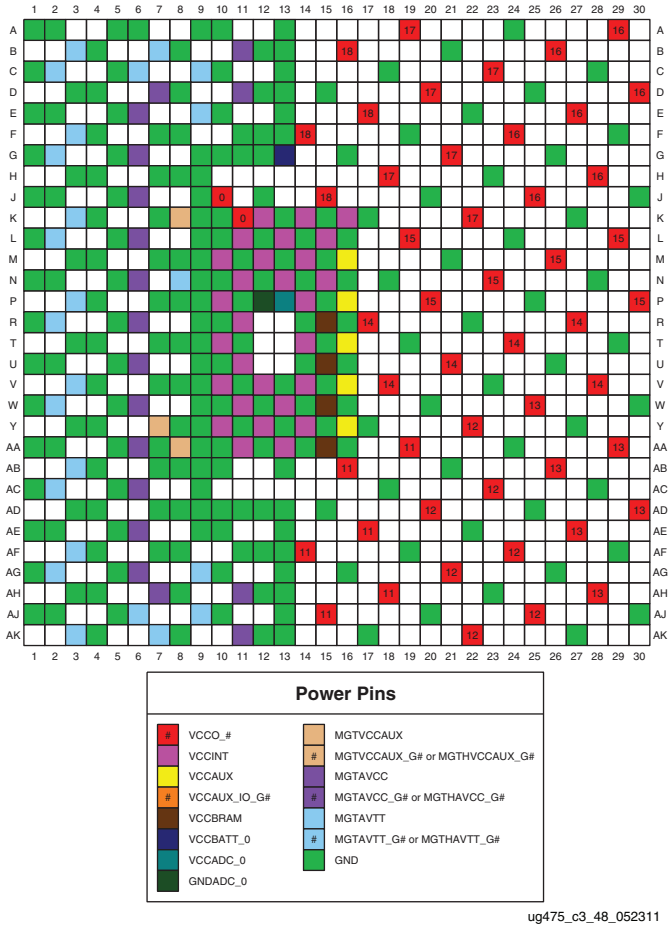


Figure 3-64: **FFG901 Package—XC7K420T and XC7K480T Power and GND Placement**

FFG1156 Package—XC7K420T and XC7K480T

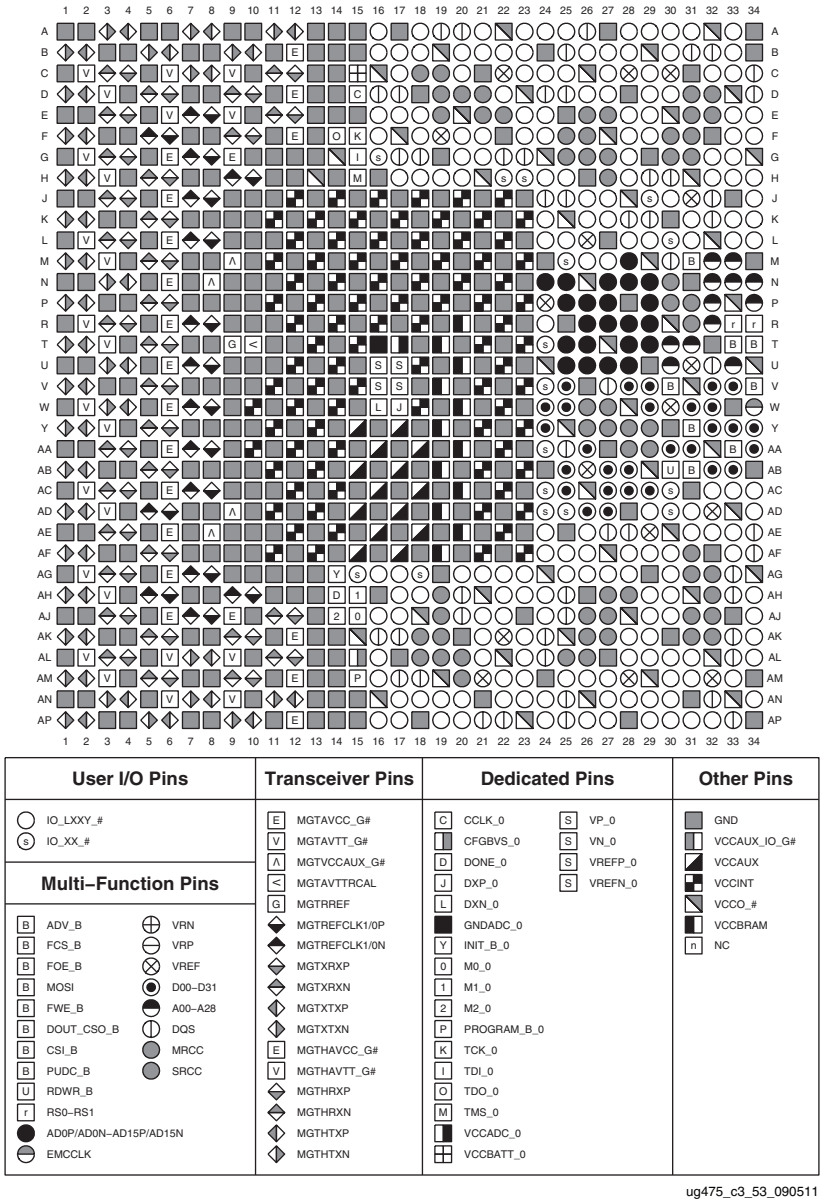


Figure 3-65: **FFG1156 Package—XC7K420T and XC7K480T Pinout Diagram**

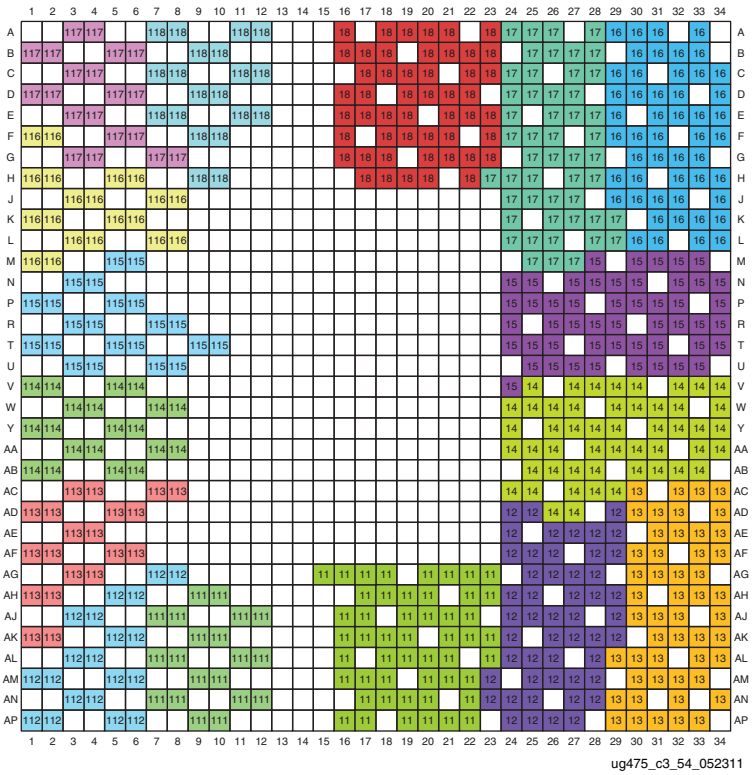


Figure 3-66: **FFG1156 Package—XC7K420T and XC7K480T I/O Banks**

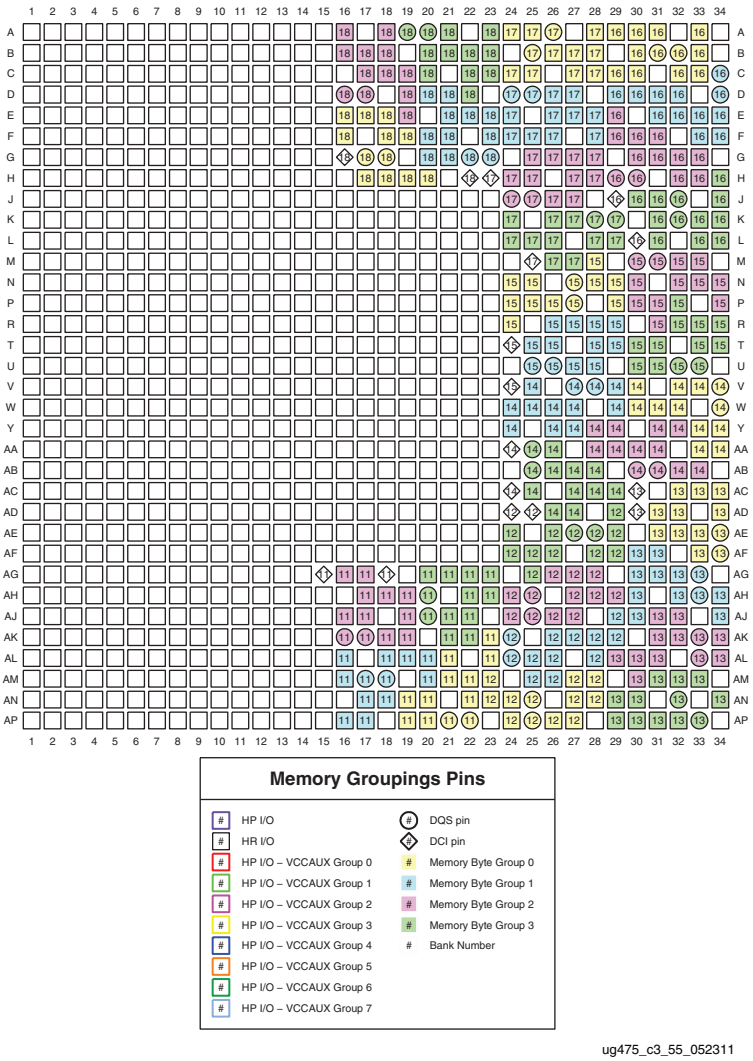


Figure 3-67: **FFG1156 Package—XC7K420T and XC7K480T Memory Groupings**

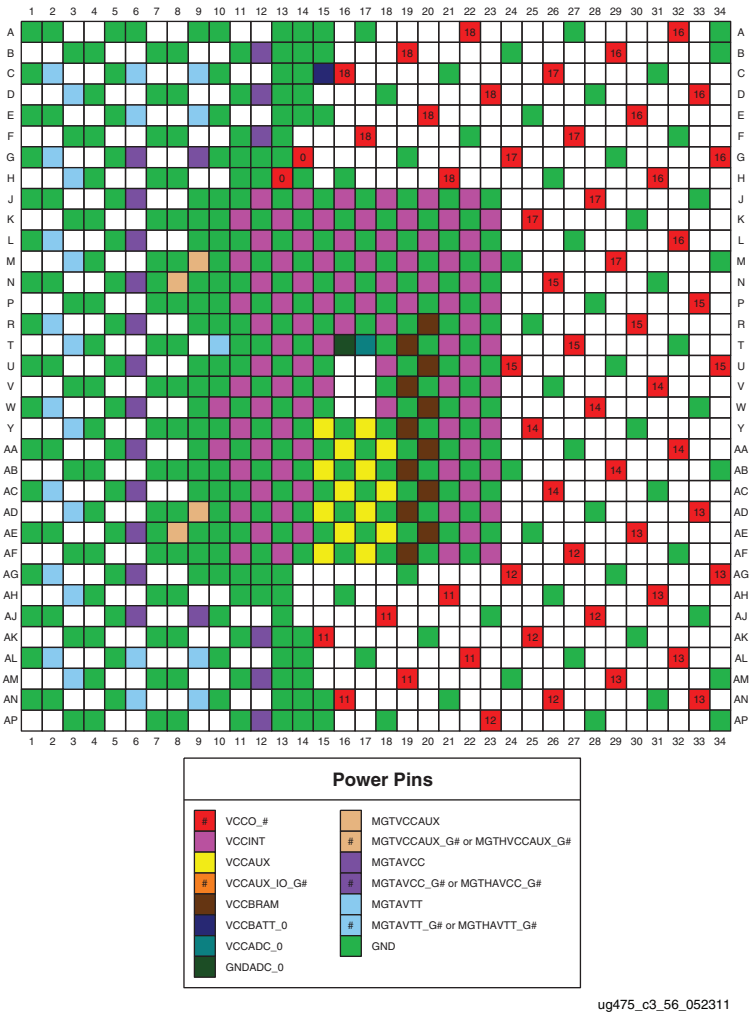


Figure 3-68: **FFG1156 Package—XC7K420T and XC7K480T Power and GND Placement**

Virtex-7 FPGAs Device Diagrams

Table 3-3: **Virtex-7 T FPGAs Device Diagrams Cross Reference**

Device	FF/FFG1157	FF/FFG1761	FL/FLG1925	FH/FHG1761
XC7V585T	page 114	page 118		
XC7V2000T			page 122	page 126

Table 3-4: **Virtex-7 XT FPGAs Device Diagrams Cross Reference**

Device	FF/FFG 1157	FF/FFG 1158	FF/FFG 1761	FF/FFG 1926	FF/FFG 1927	FF/FFG 1928	FF/FFG 1930	FL/FLG 1926	FL/FLG 1928	FL/FLG 1930
XC7VX330T	page 130		page 134							
XC7VX415T	page 130	page 138			page 142					
XC7VX485T	page 146	page 150	page 154		page 158		page 162			
XC7VX550T		page 138			page 174					
XC7VX690T	page 130	page 138	page 166	page 170	page 174		page 178			
XC7VX980T				page 170		page 182	page 186			
XC7VX1140T								page 190	page 194	page 198

Table 3-5: **Virtex-7 HT FPGAs Device Diagrams Cross Reference**

Device	HC/HCG1155	HC/HCG1931	HC/HCG1932
XC7VH580T	page 202	page 206	page 210
XC7VH870T		page 214	page 218

FFG1157 Package—XC7V585T

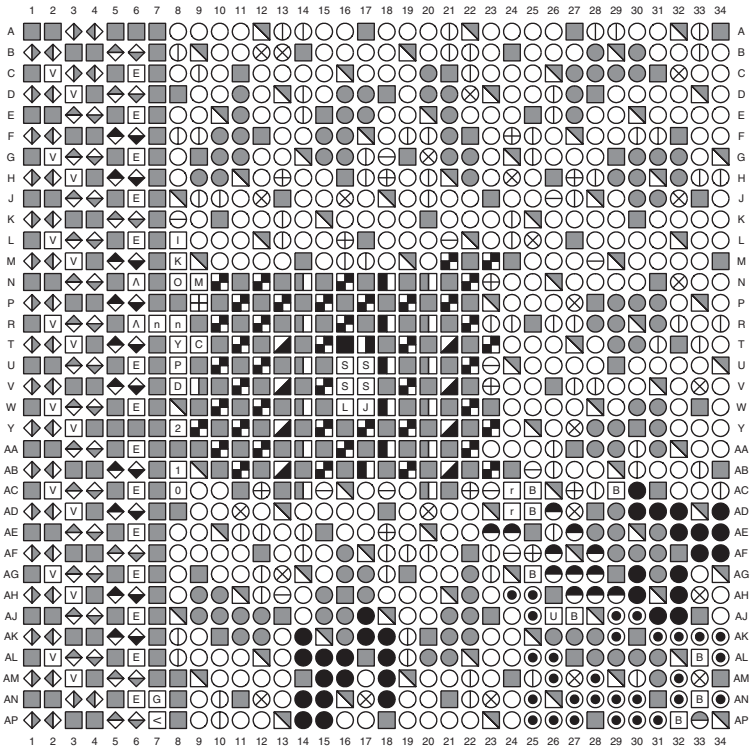


Figure 3-69: **FFG1157 Package—XC7V585T Pinout Diagram**

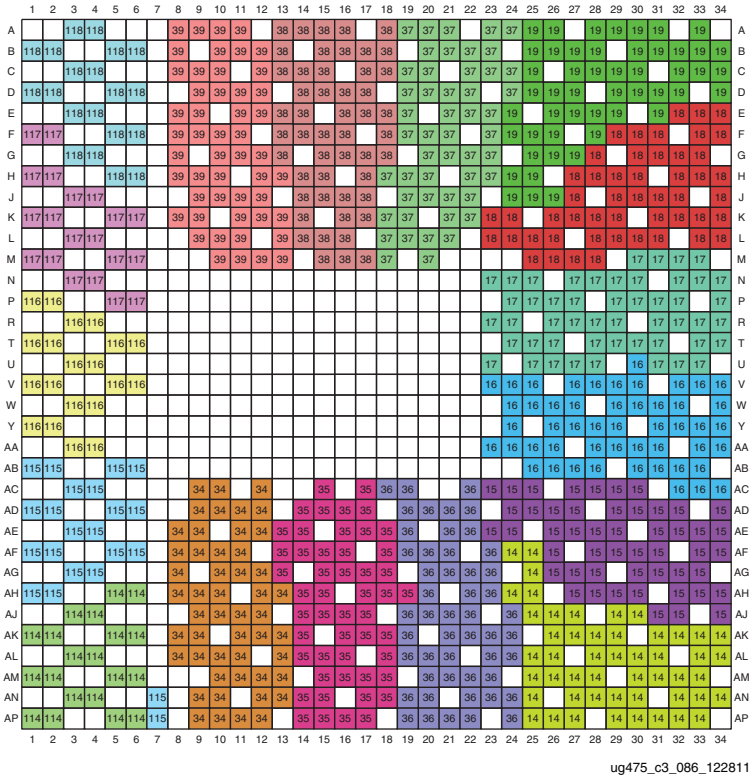


Figure 3-70: **FFG1157 Package—XC7V585T I/O Banks**

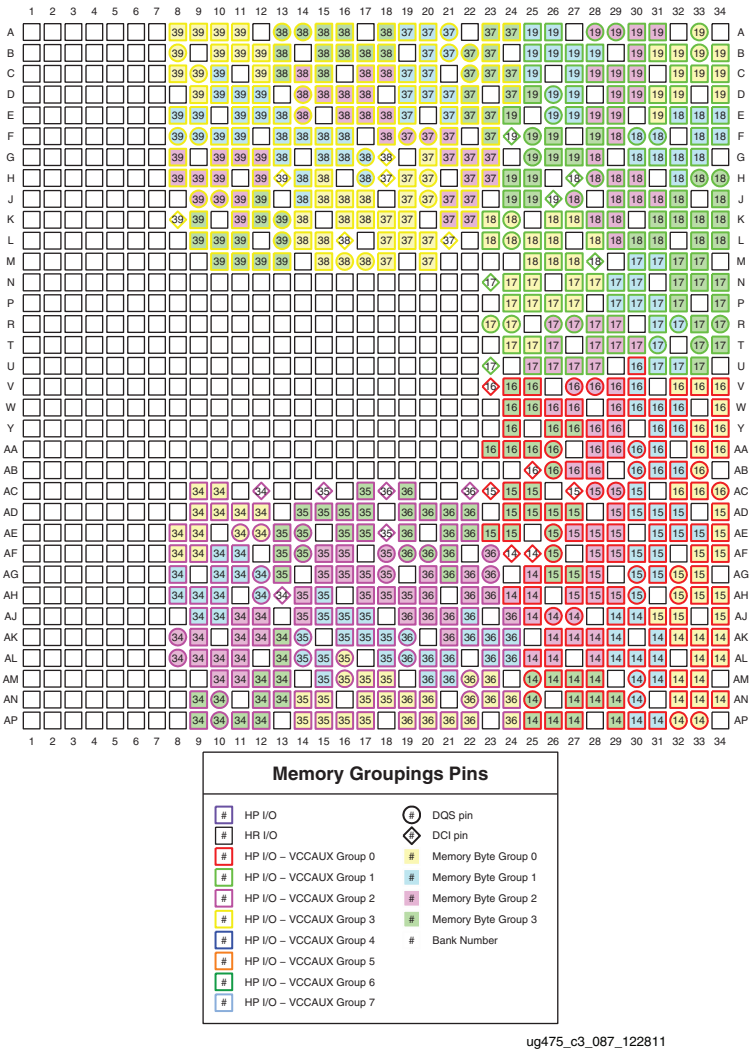


Figure 3-71: **FFG1157 Package—XC7V585T Memory Groupings**

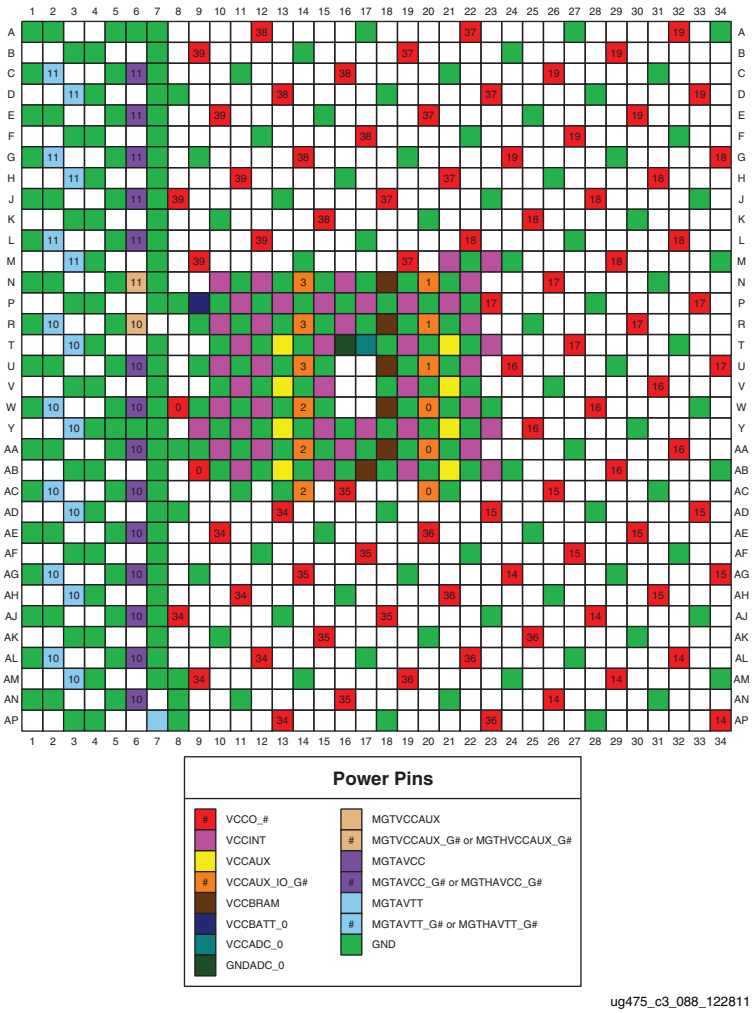


Figure 3-72: **FFG1157 Package—XC7V585T Power and GND Placement**

FFG1761 Package—XC7V585T

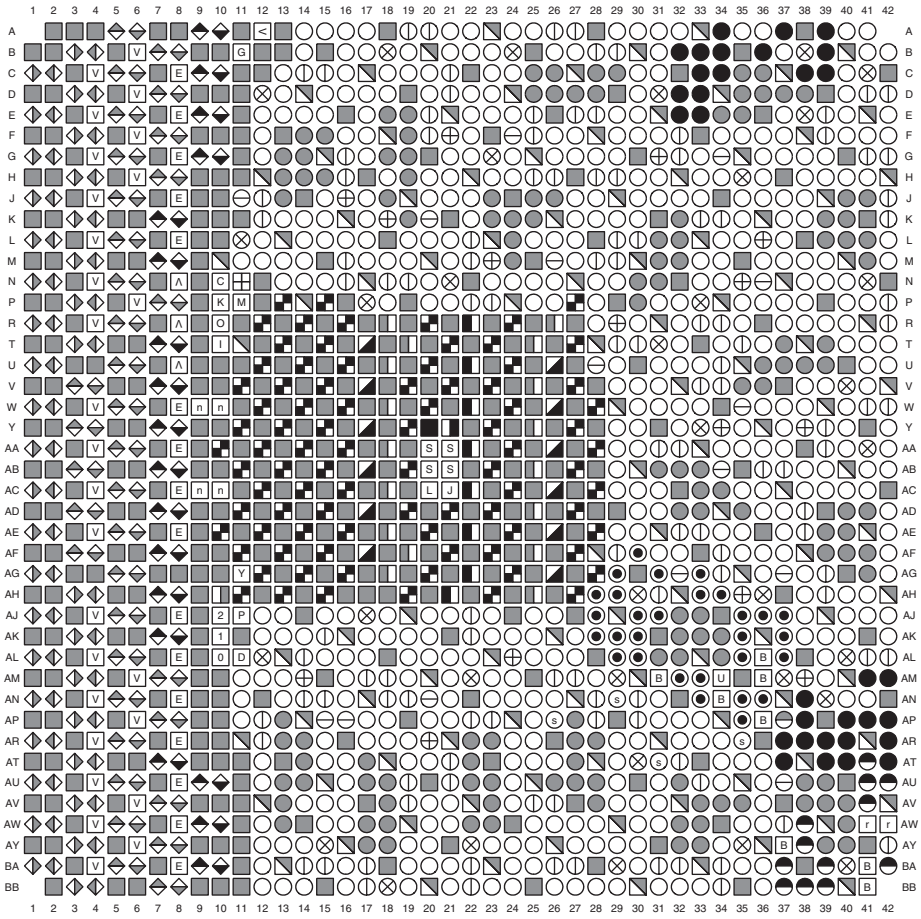


Figure 3-73: **FFG1761 Package—XC7V585T Pinout Diagram**

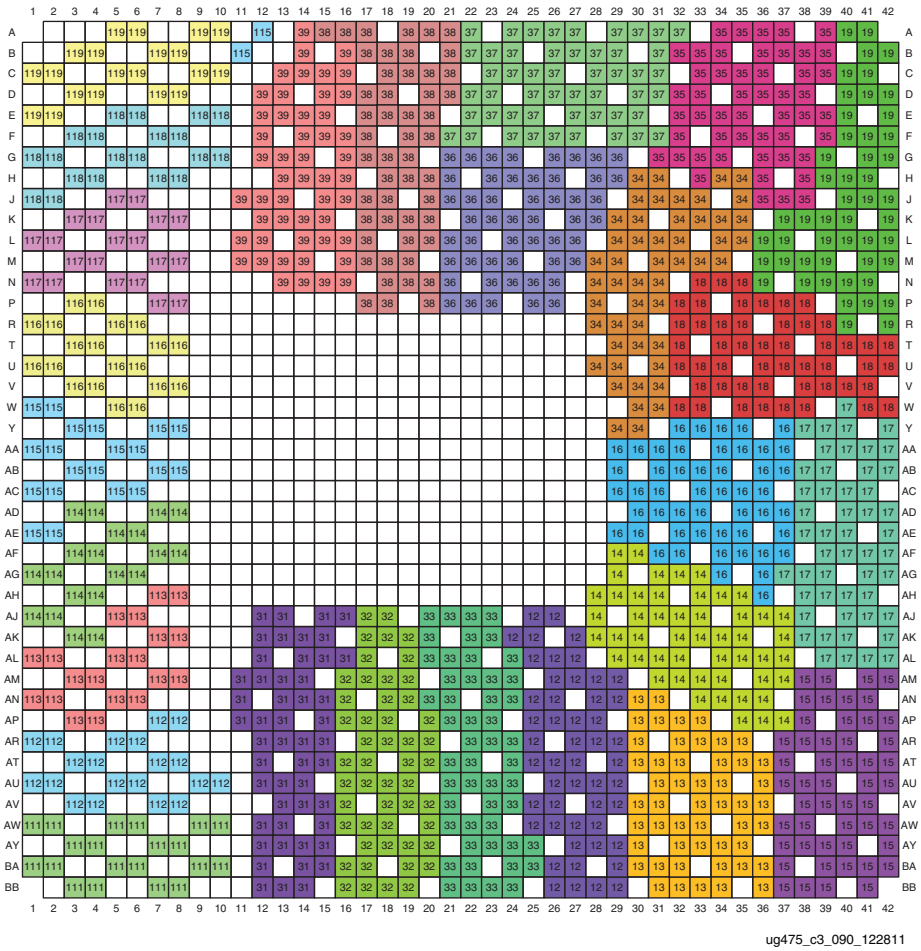


Figure 3-74: **FFG1761 Package—XC7V585T I/O Banks**

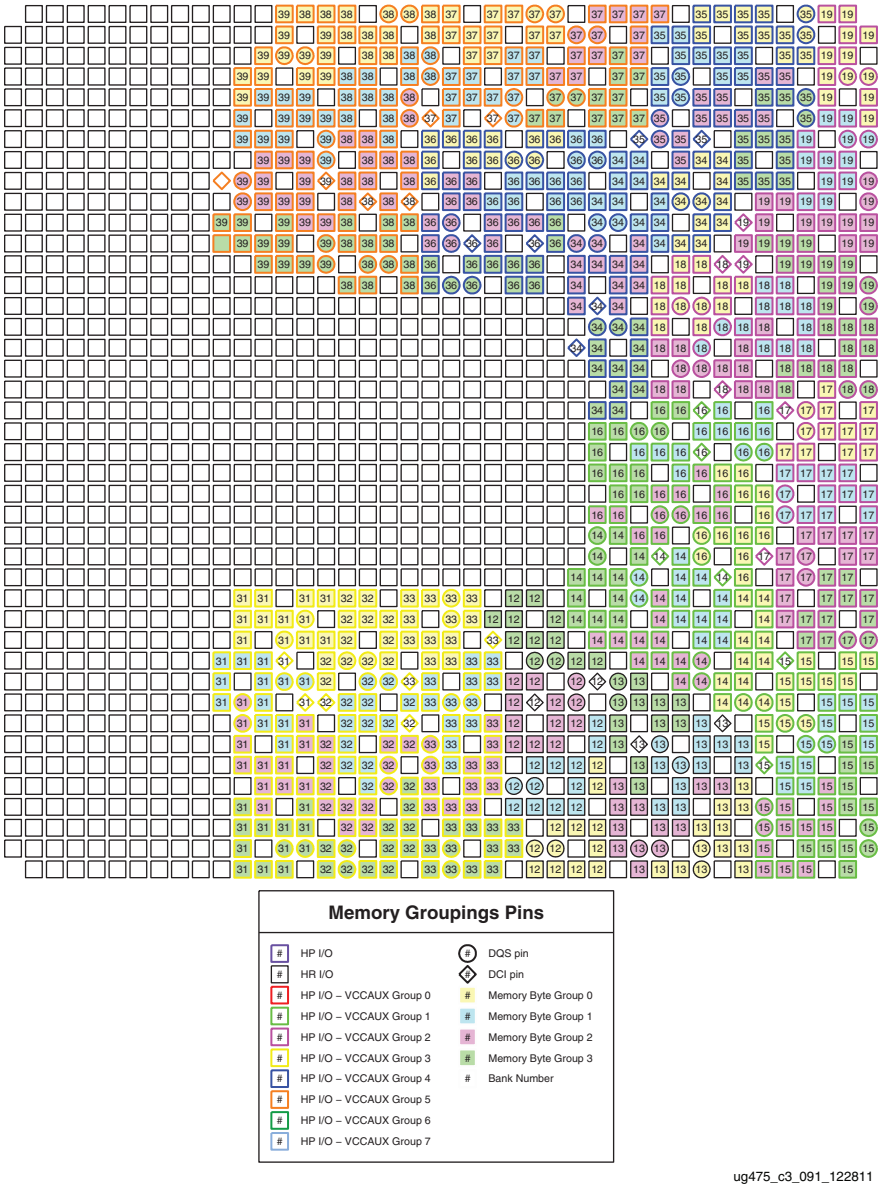


Figure 3-75: **FFG1761 Package—XC7V585T Memory Groupings**

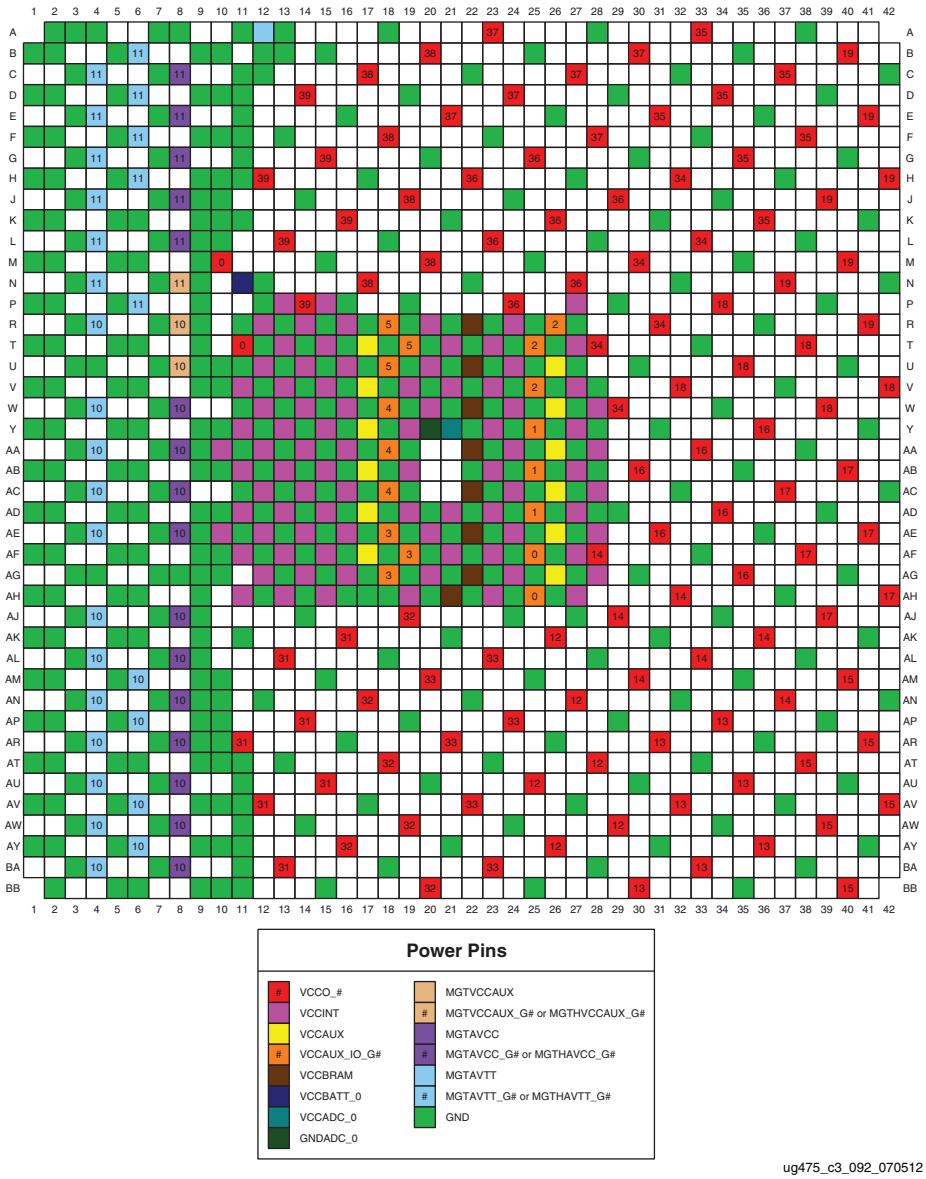


Figure 3-76: **FFG1761 Package—XC7V585T Power and GND Placement**

FLG1925 Package—XC7V2000T

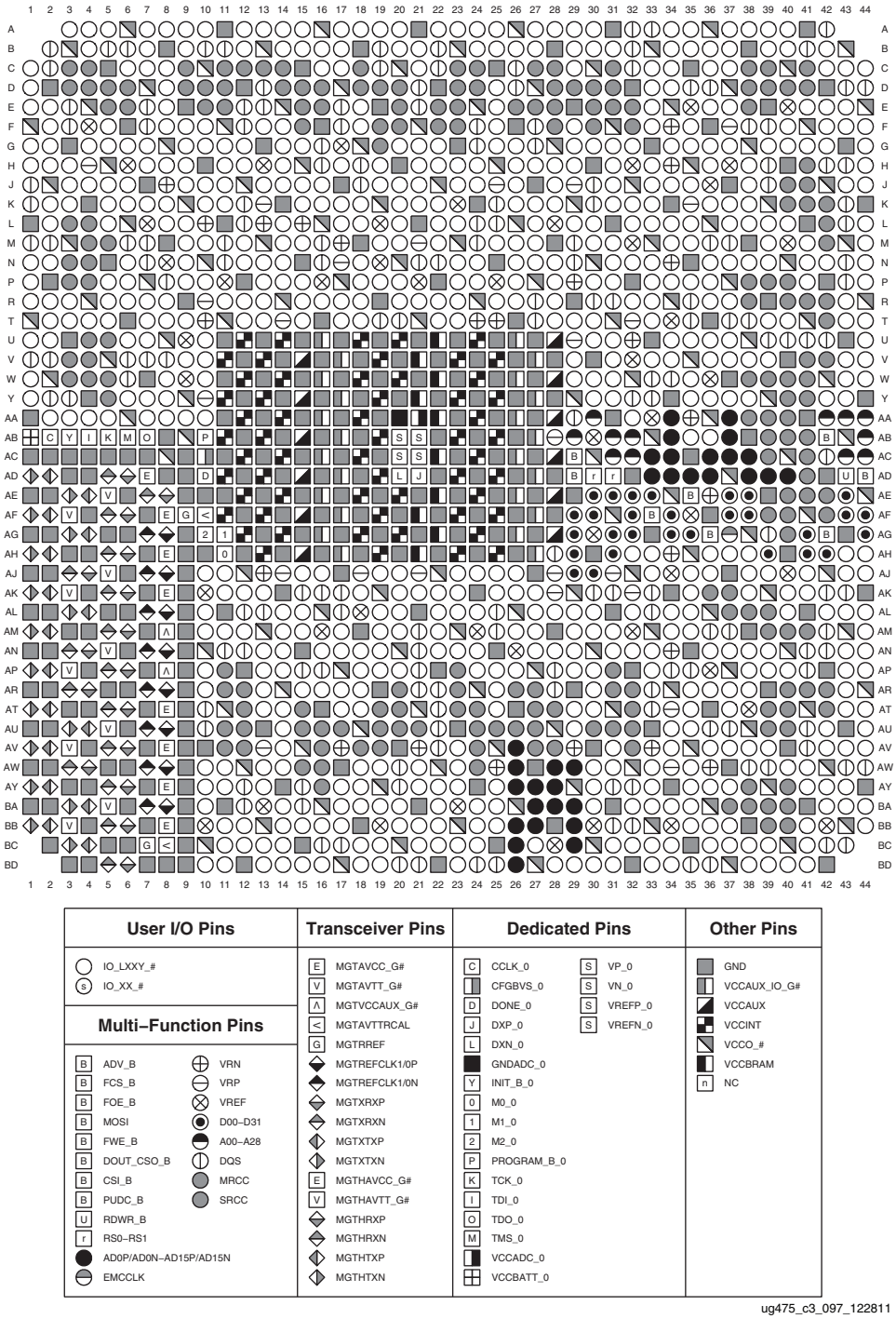


Figure 3-77: **FLG1925 Package—XC7V2000T Pinout Diagram**

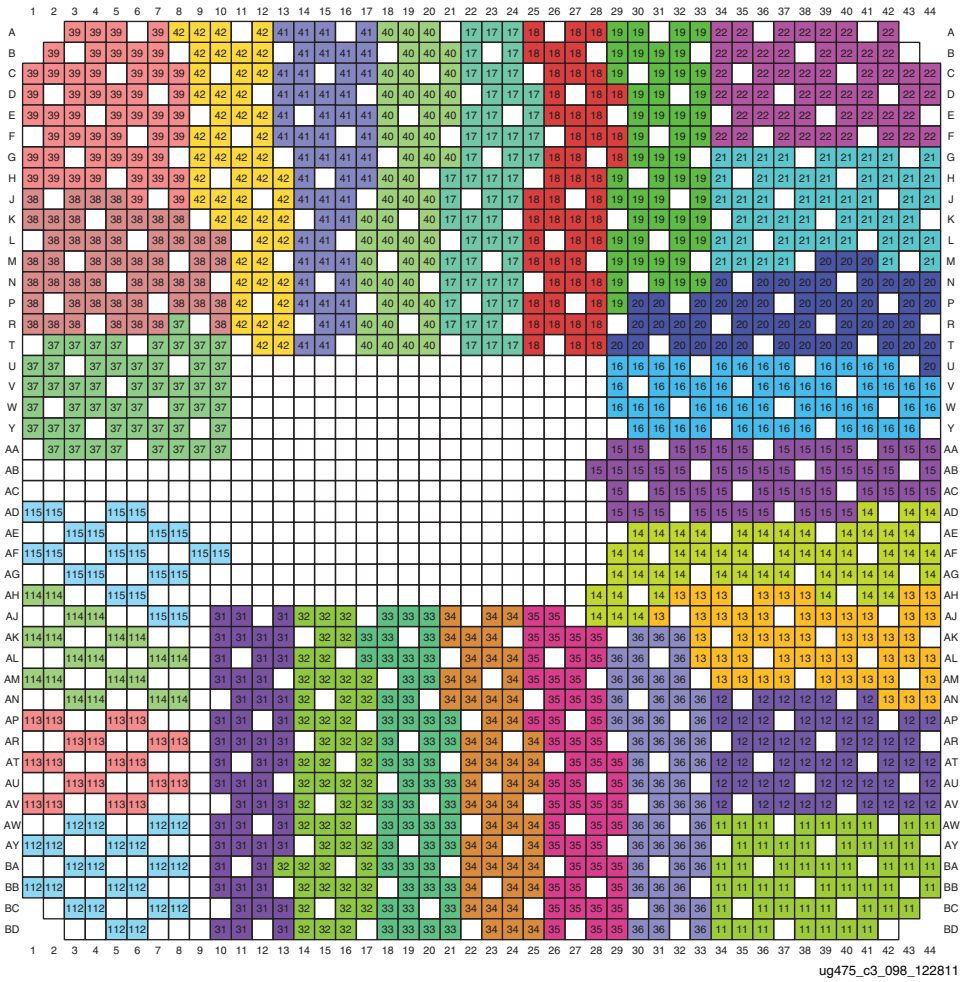


Figure 3-78: **FLG1925 Package—XC7V2000T I/O Banks**

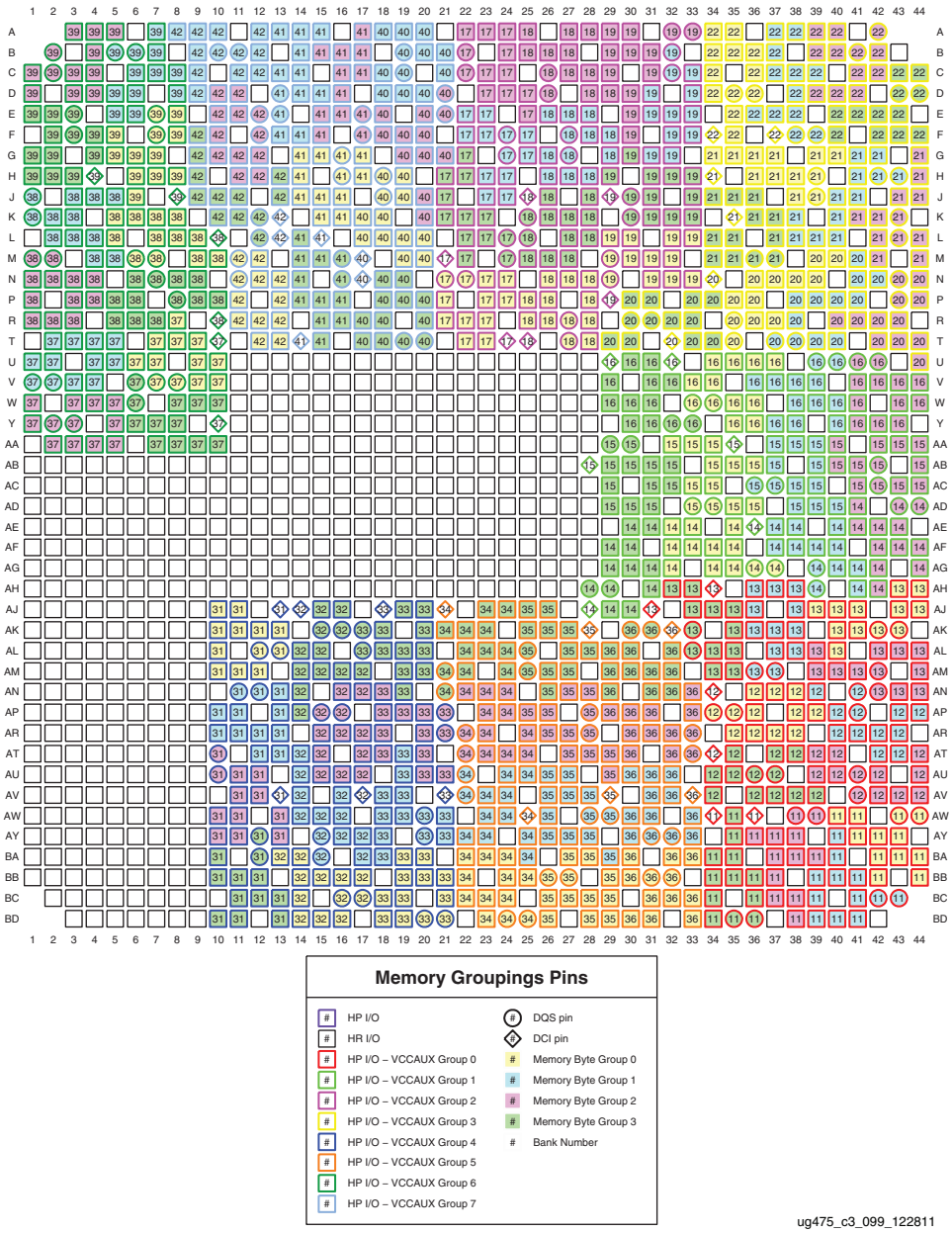


Figure 3-79: **FLG1925 Package—XC7V2000T Memory Groupings**

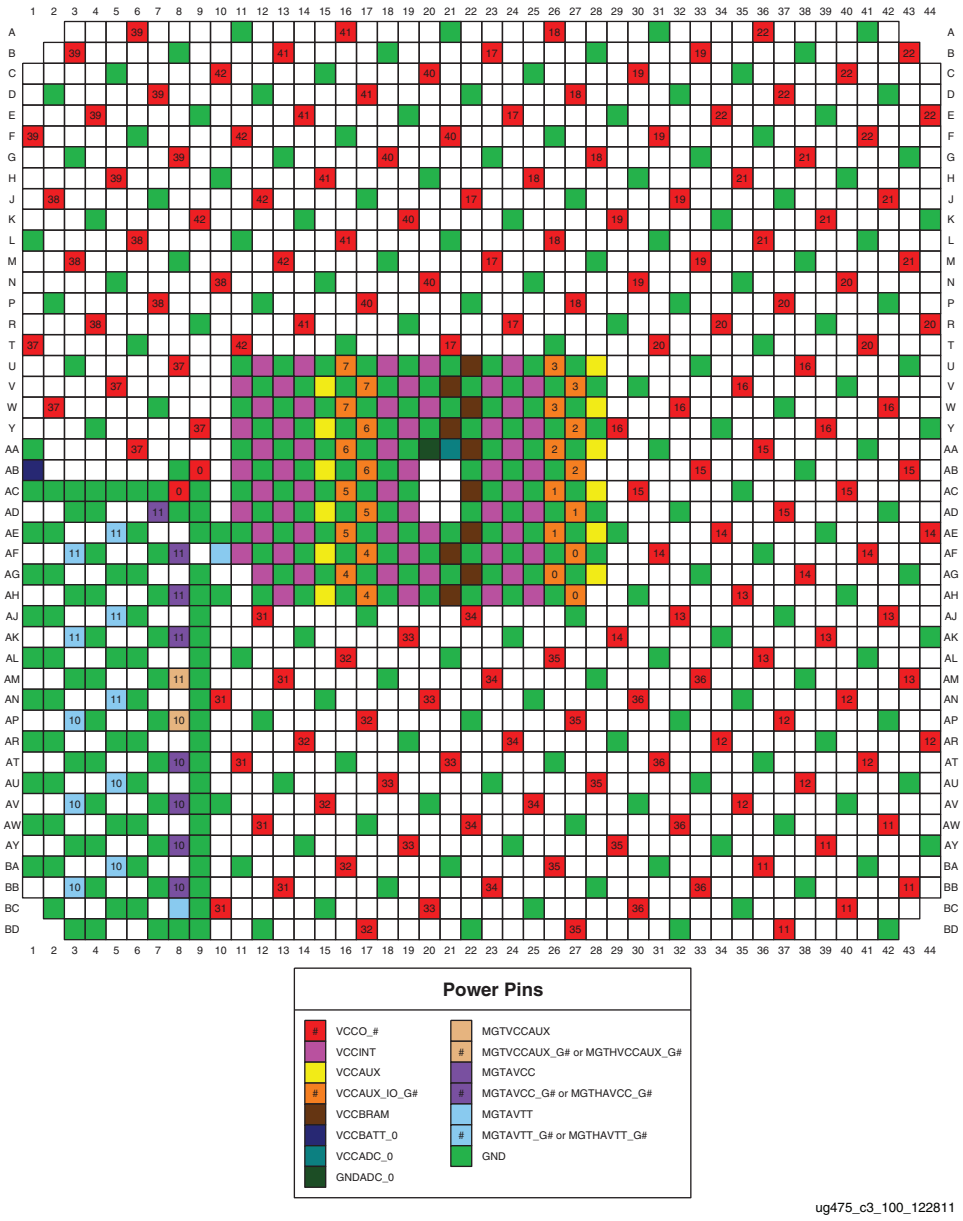


Figure 3-80: **FLG1925 Package—XC7V2000T Power and GND Placement**

FHG1761 Package—XC7V2000T

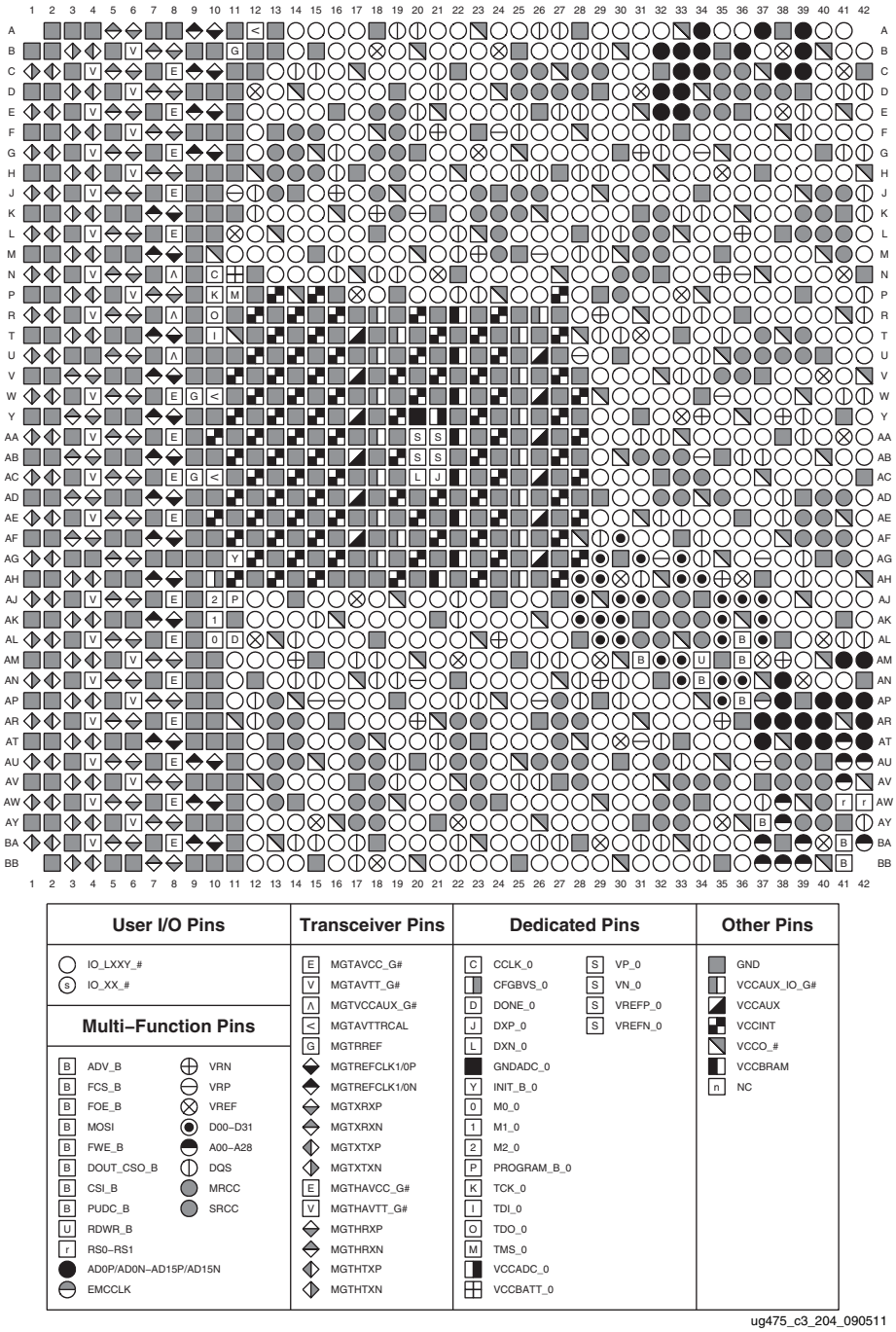


Figure 3-81: **FHG1761 Package—XC7V2000T Pinout Diagram**

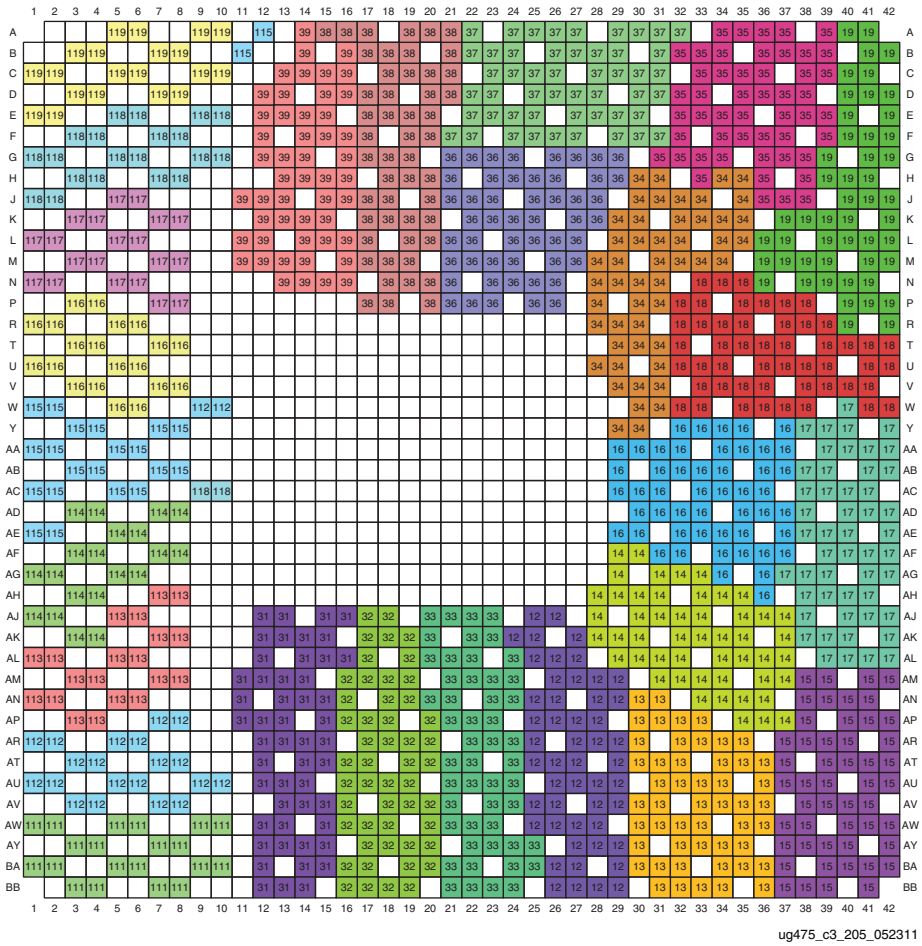


Figure 3-82: **FHG1761 Package—XC7V2000T I/O Banks**

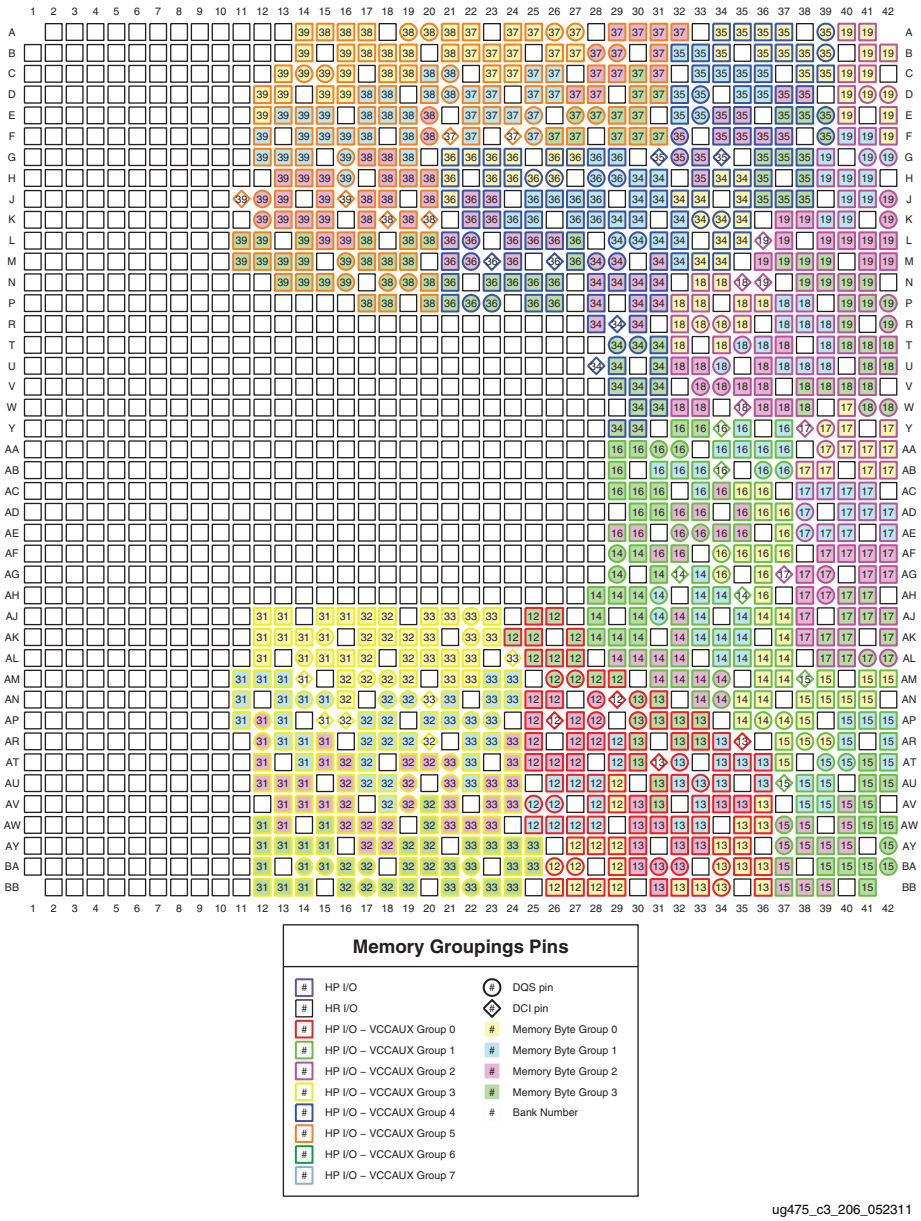


Figure 3-83: **FHG1761 Package—XC7V2000T Memory Groupings**

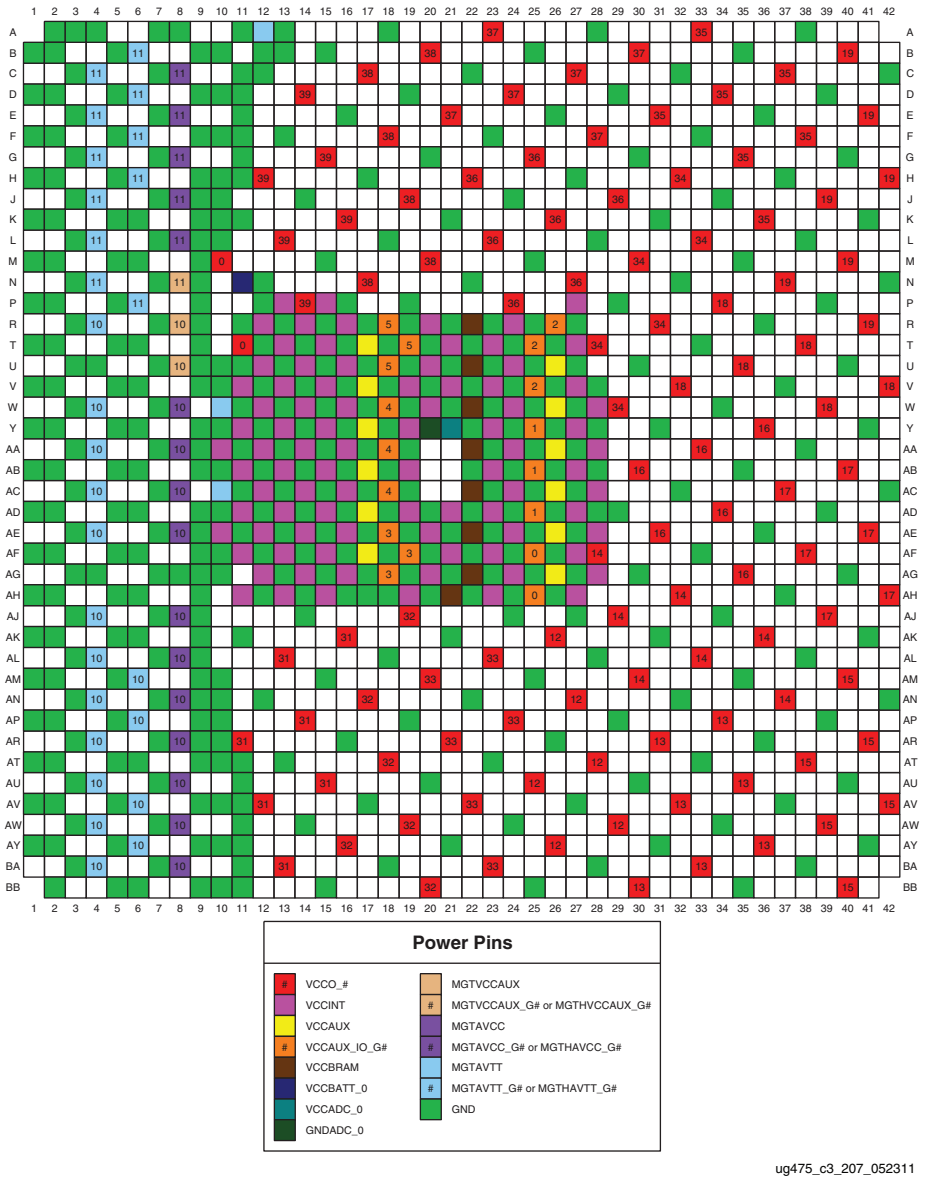


Figure 3-84: **FHG1761 Package—XC7V2000T Power and GND Placement**

FFG1157 Package—XC7VX330T, XC7VX415T, and XC7VX690T

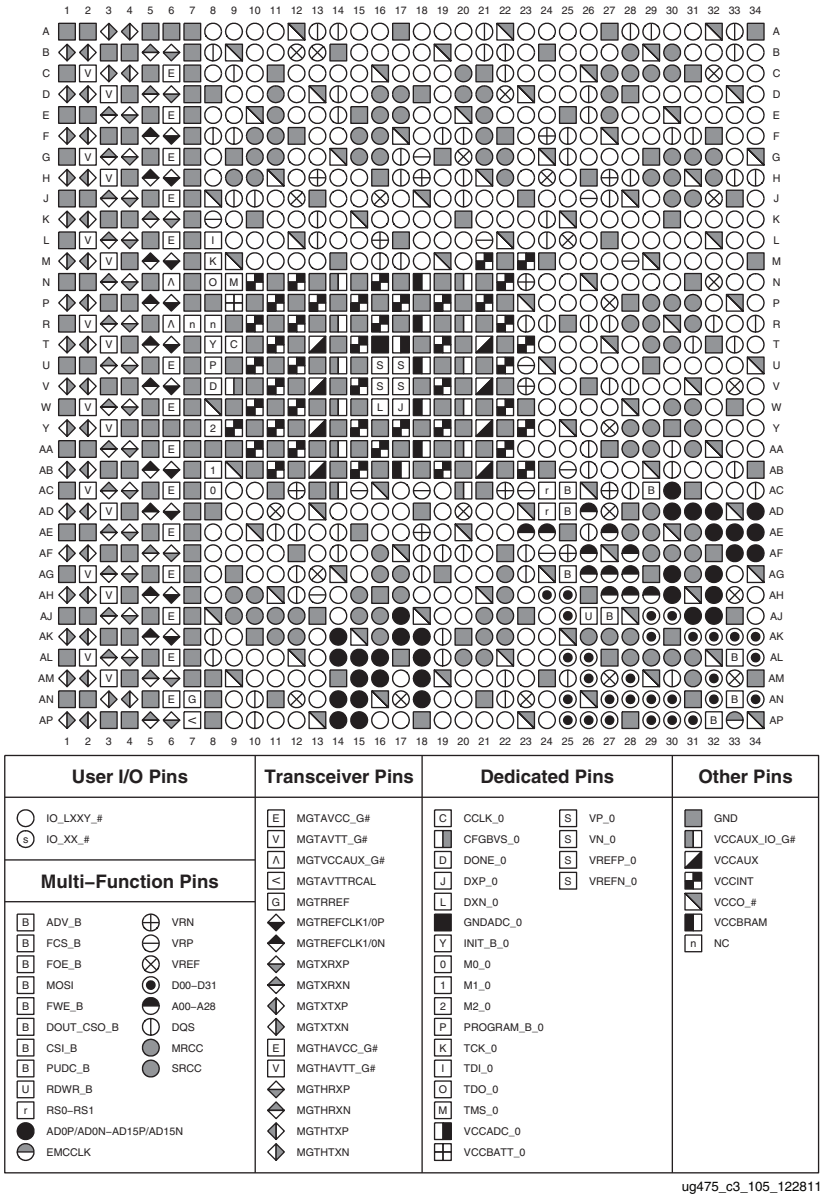


Figure 3-85: **FFG1157 Package—XC7VX330T, XC7VX415T, and XC7VX690T Pinout Diagram**

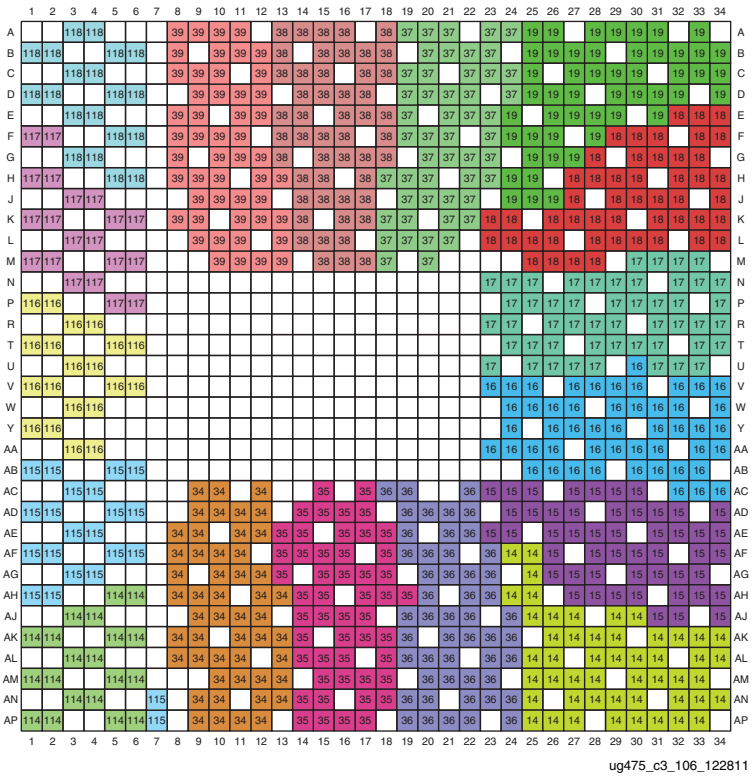


Figure 3-86: **FFG1157 Package—XC7VX330T, XC7VX415T, and XC7VX690T I/O Banks**

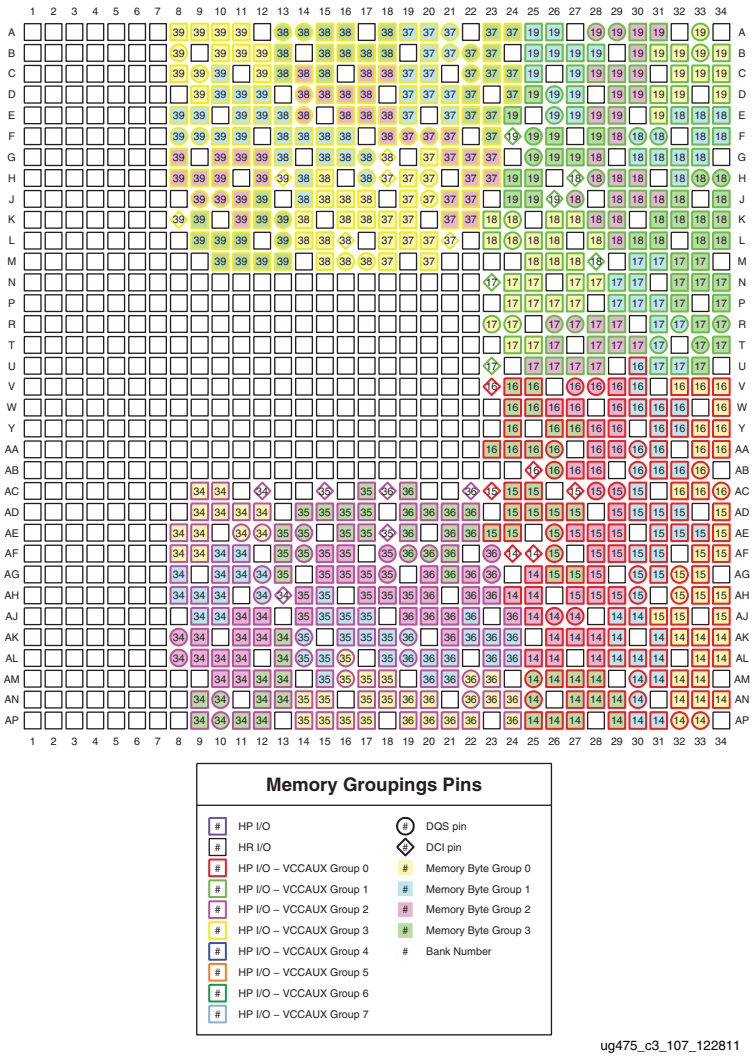


Figure 3-87: **FFG1157 Package—XC7VX330T, XC7VX415T, and XC7VX690T Memory Groupings**

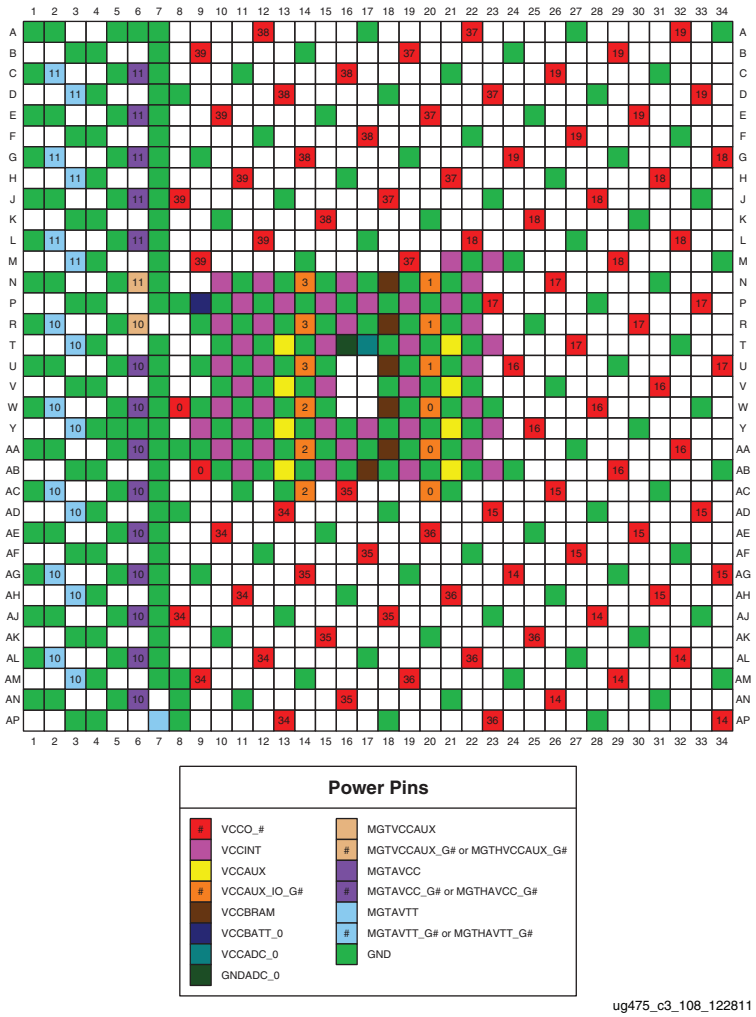


Figure 3-88: **FFG1157 Package—XC7VX330T, XC7VX415T, and XC7VX690T Power and GND Placement**

FFG1761 Package—XC7VX330T

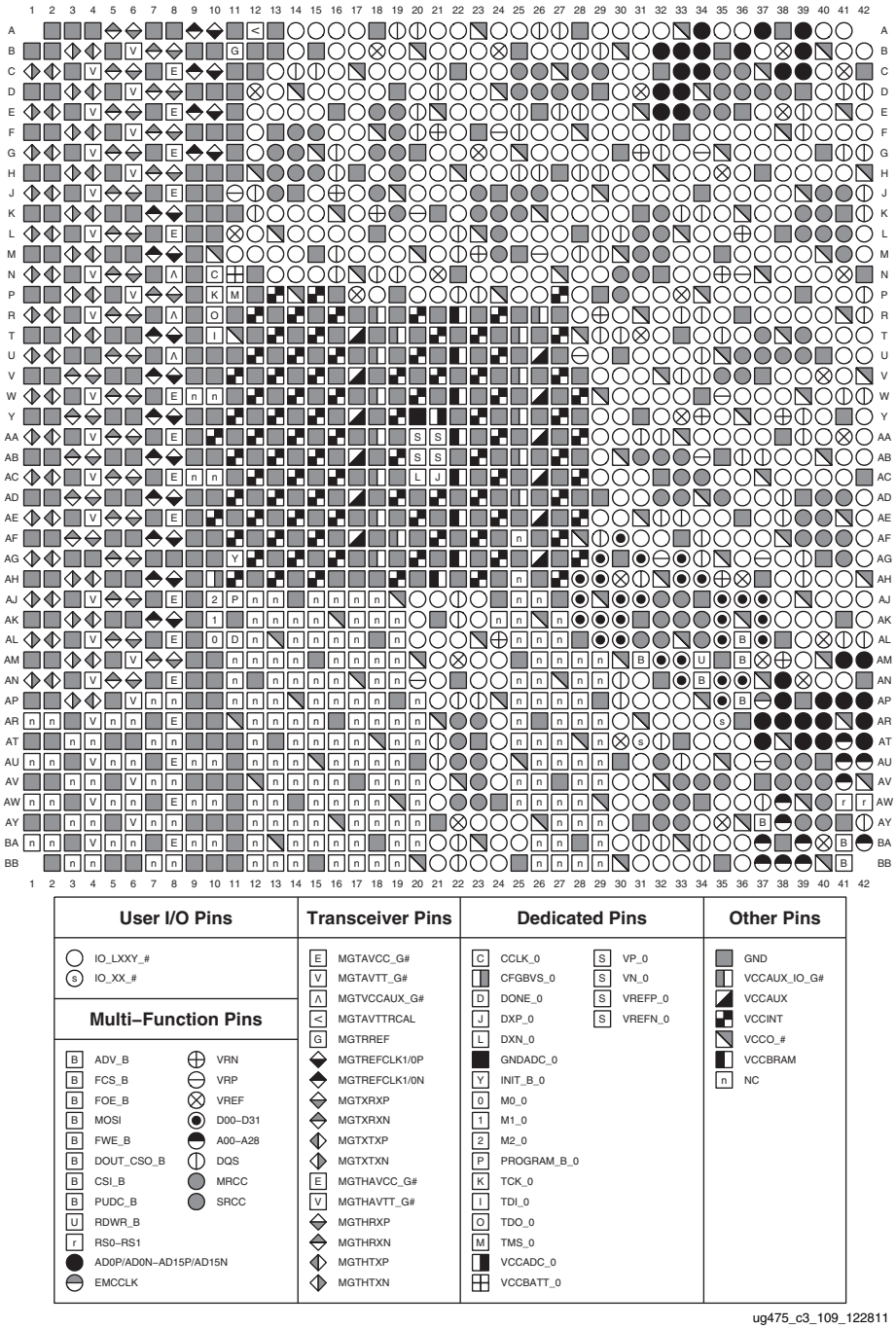


Figure 3-89: **FFG1761 Package—XC7VX330T Pinout Diagram**

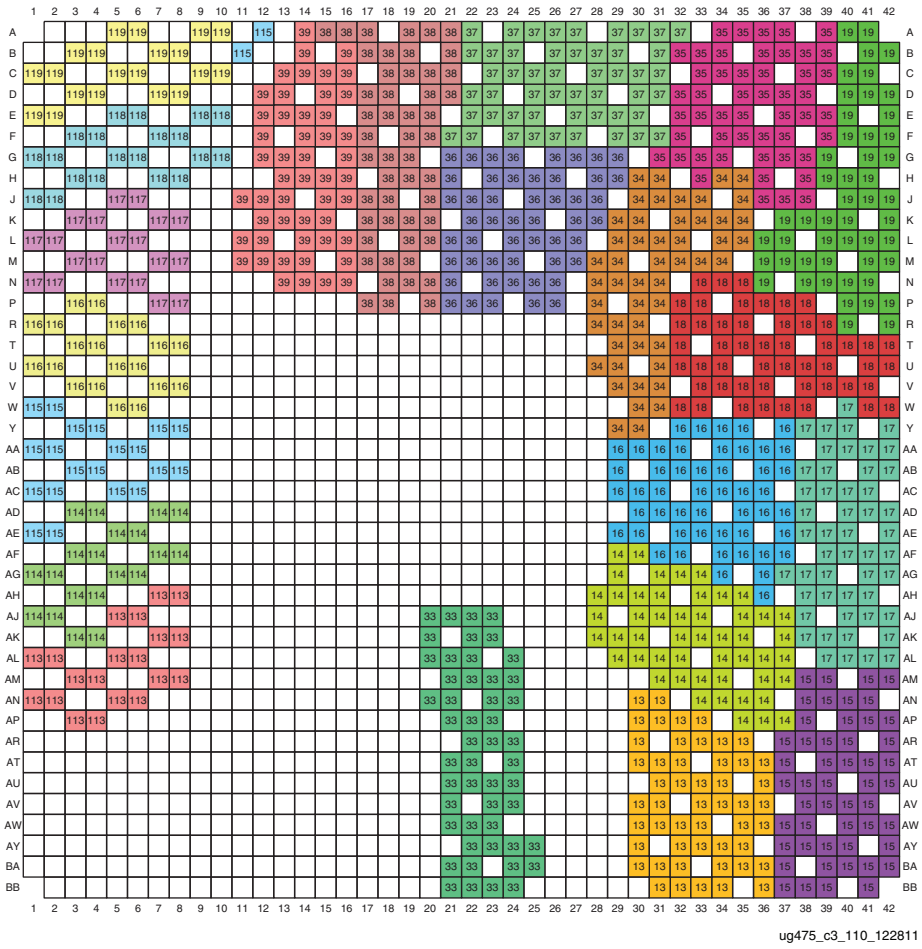


Figure 3-90: **FFG1761 Package—XC7VX330T I/O Banks**

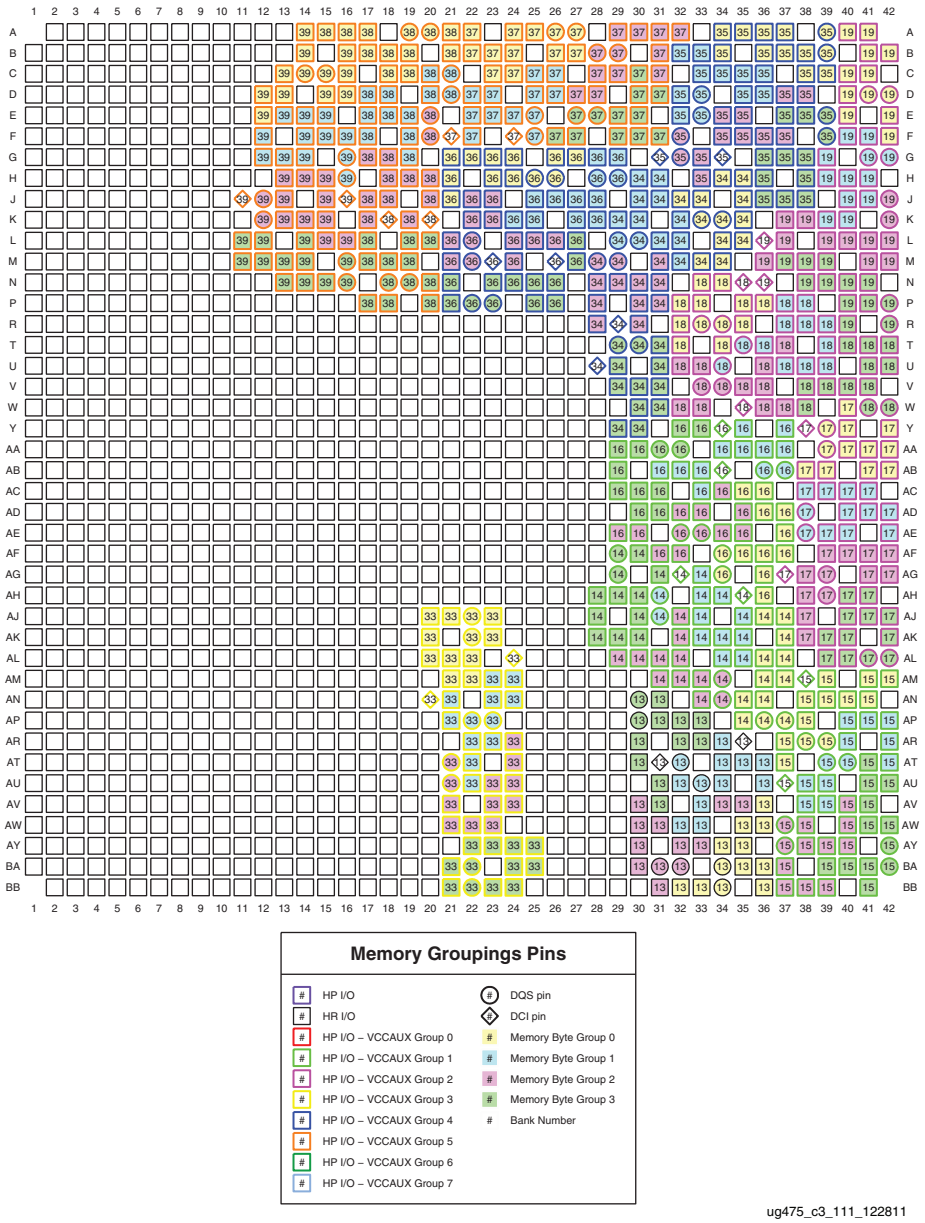


Figure 3-91: **FFG1761 Package—XC7VX330T Memory Groupings**

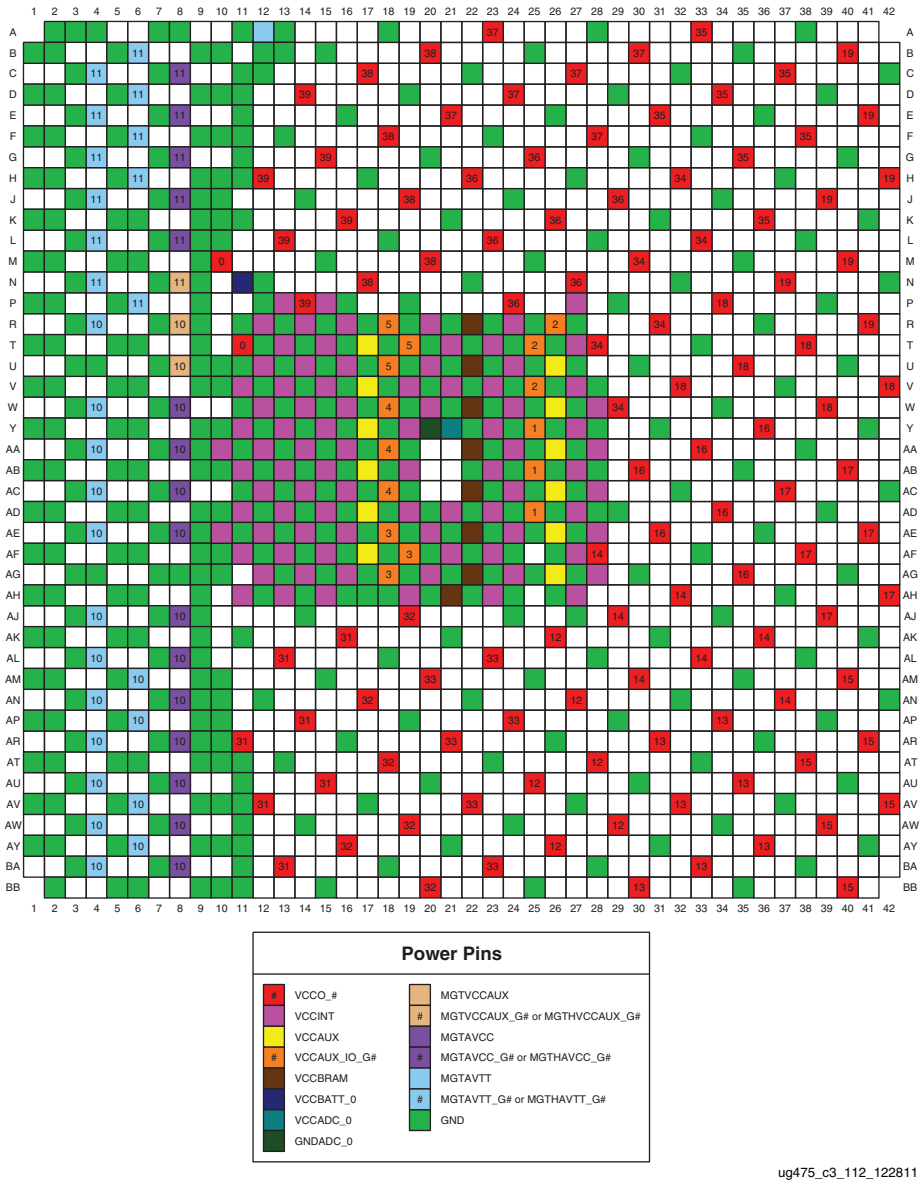


Figure 3-92: **FFG1761 Package—XC7VX330T Power and GND Placement**

FFG1158 Package—XC7VX415T, XC7VX550T, and XC7VX690T

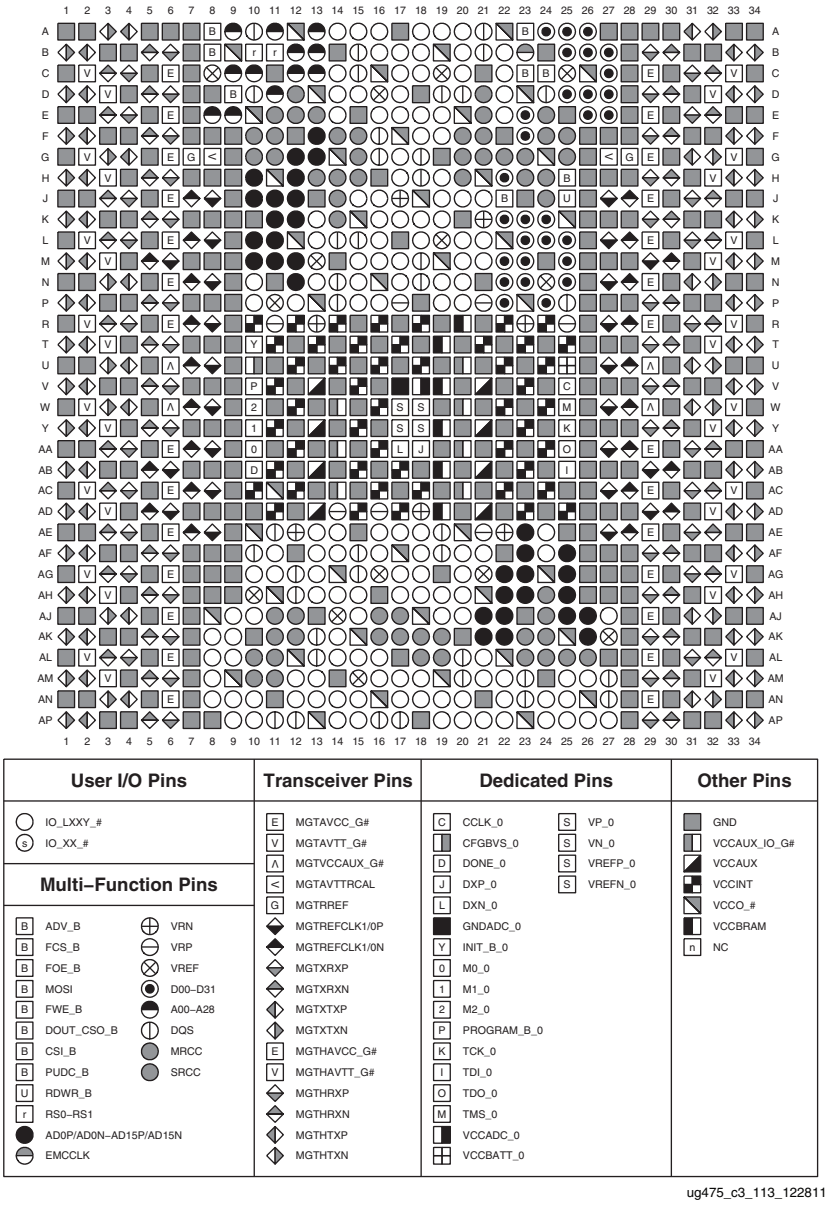


Figure 3-93: **FFG1158 Package—XC7VX415T, XC7VX550T, and XC7VX690T Pinout Diagram**

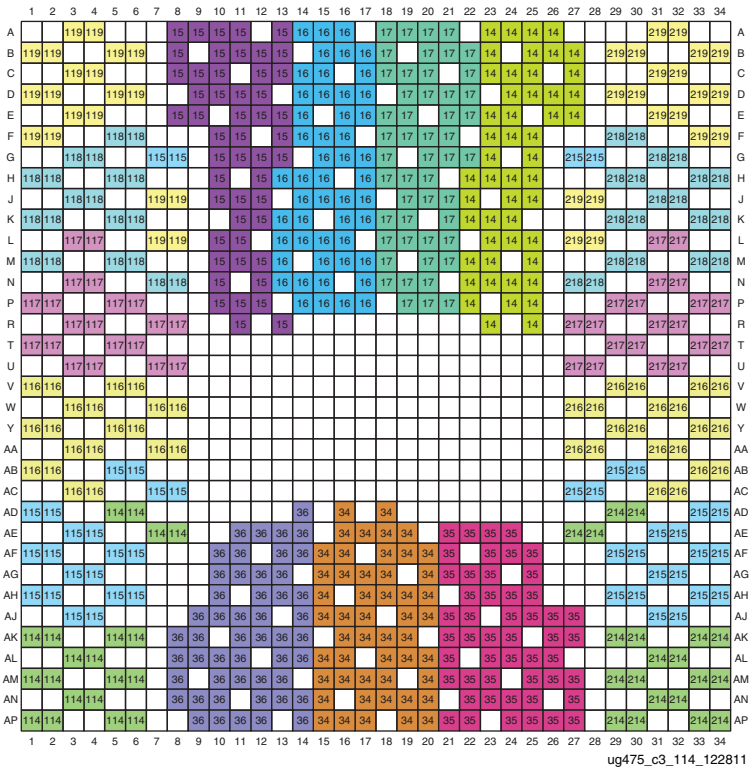


Figure 3-94: **FFG1158 Package—XC7VX415T, XC7VX550T, and XC7VX690T I/O Banks**

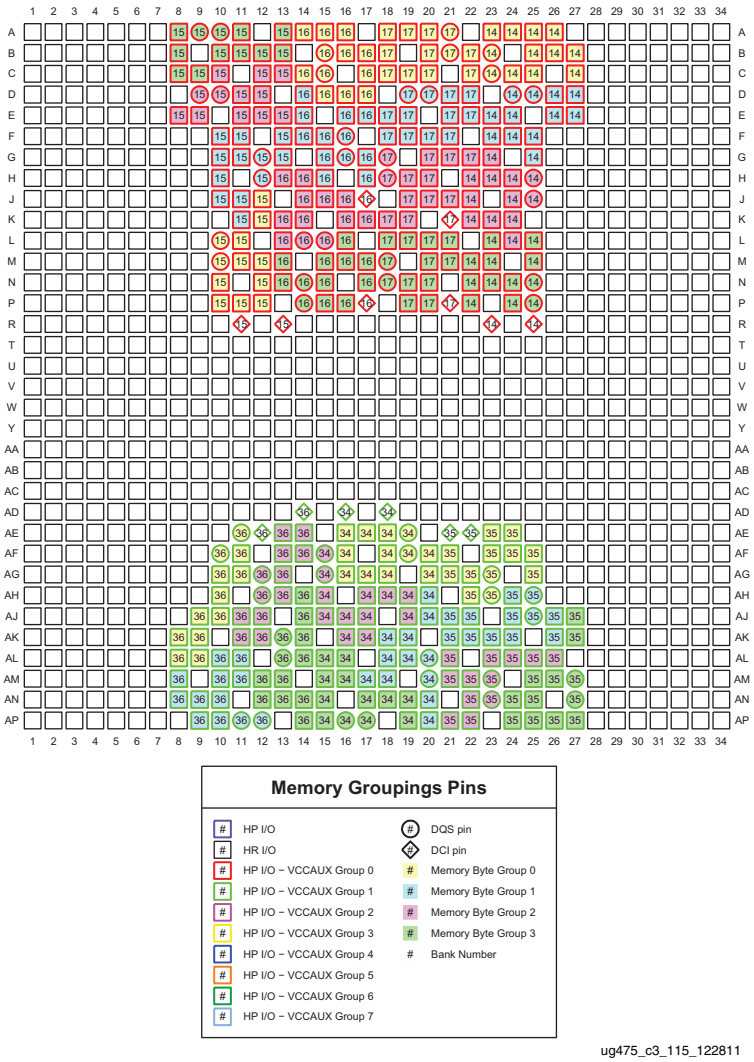


Figure 3-95: **FFG1158 Package—XC7VX415T, XC7VX550T, and XC7VX690T Memory Groupings**

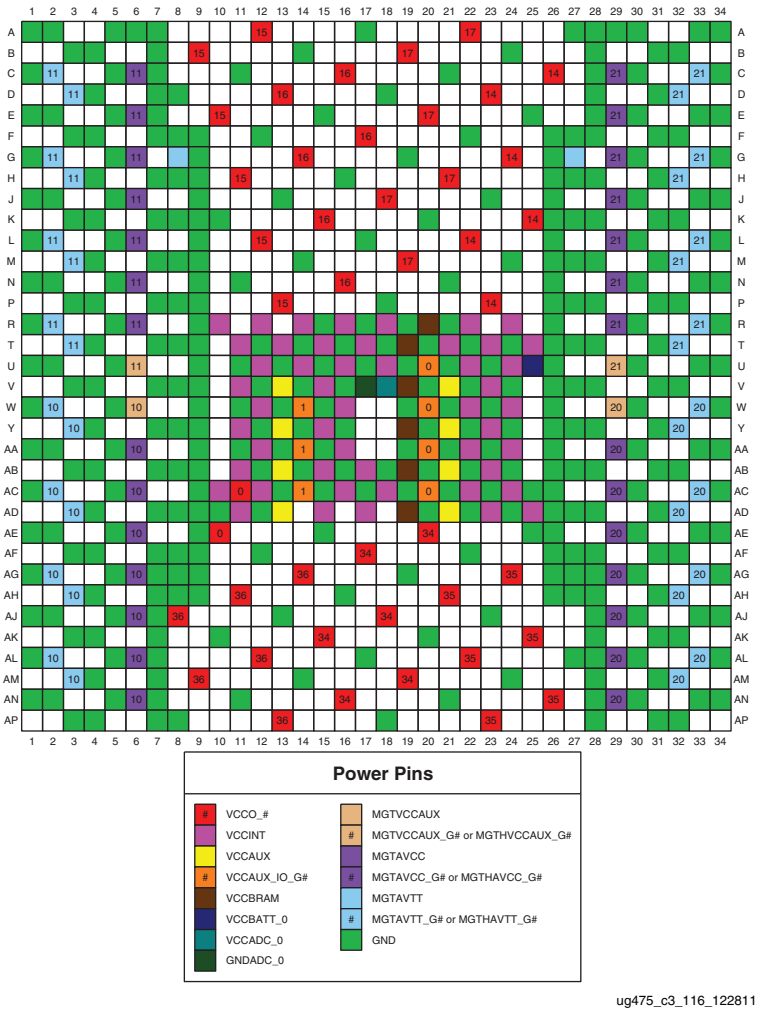


Figure 3-96: **FFG1158 Package—XC7VX415T, XC7VX550T, and XC7VX690T Power and GND Placement**

FFG1927 Package—XC7VX415T

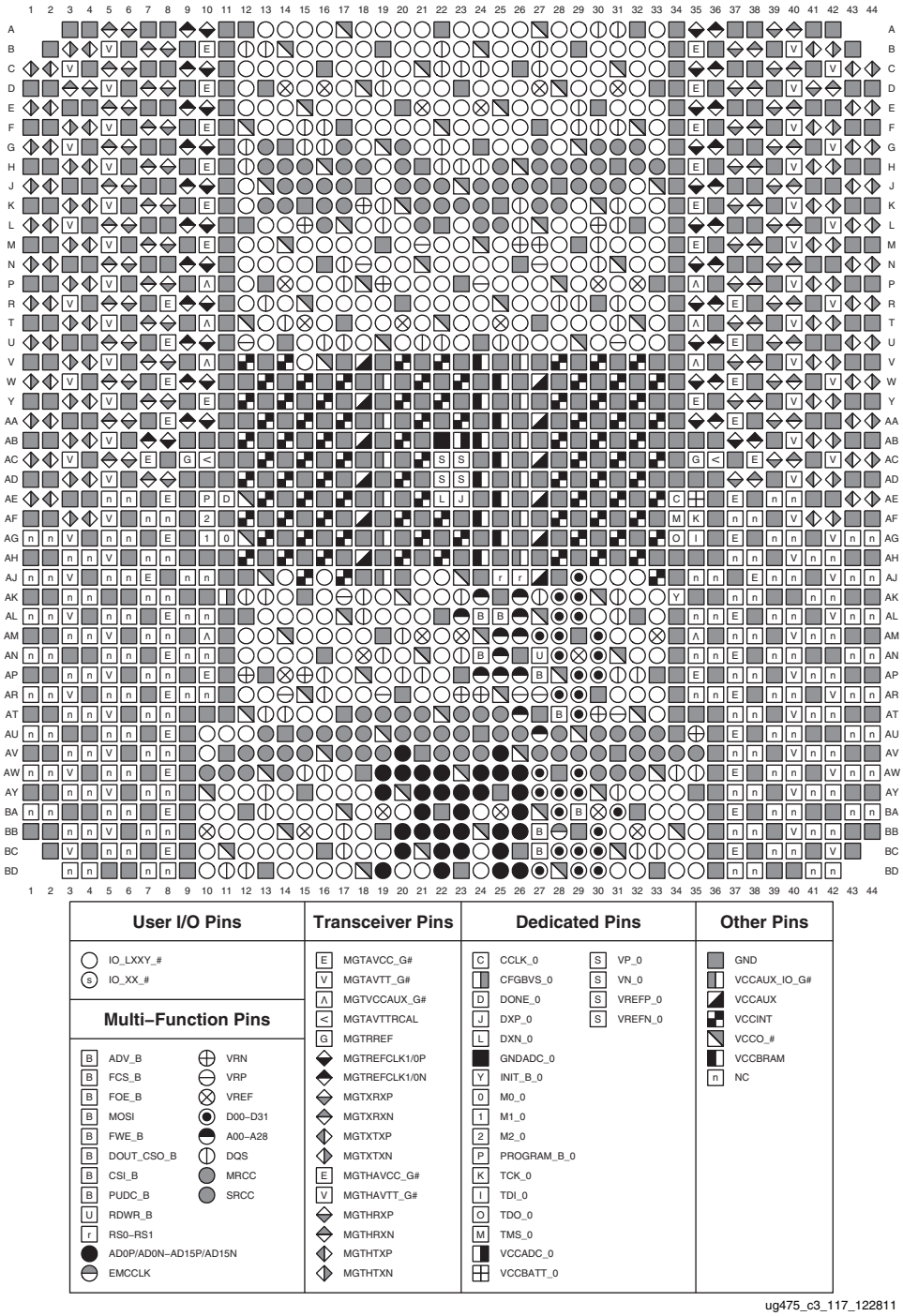


Figure 3-97: **FFG1927 Package—XC7VX415T Pinout Diagram**

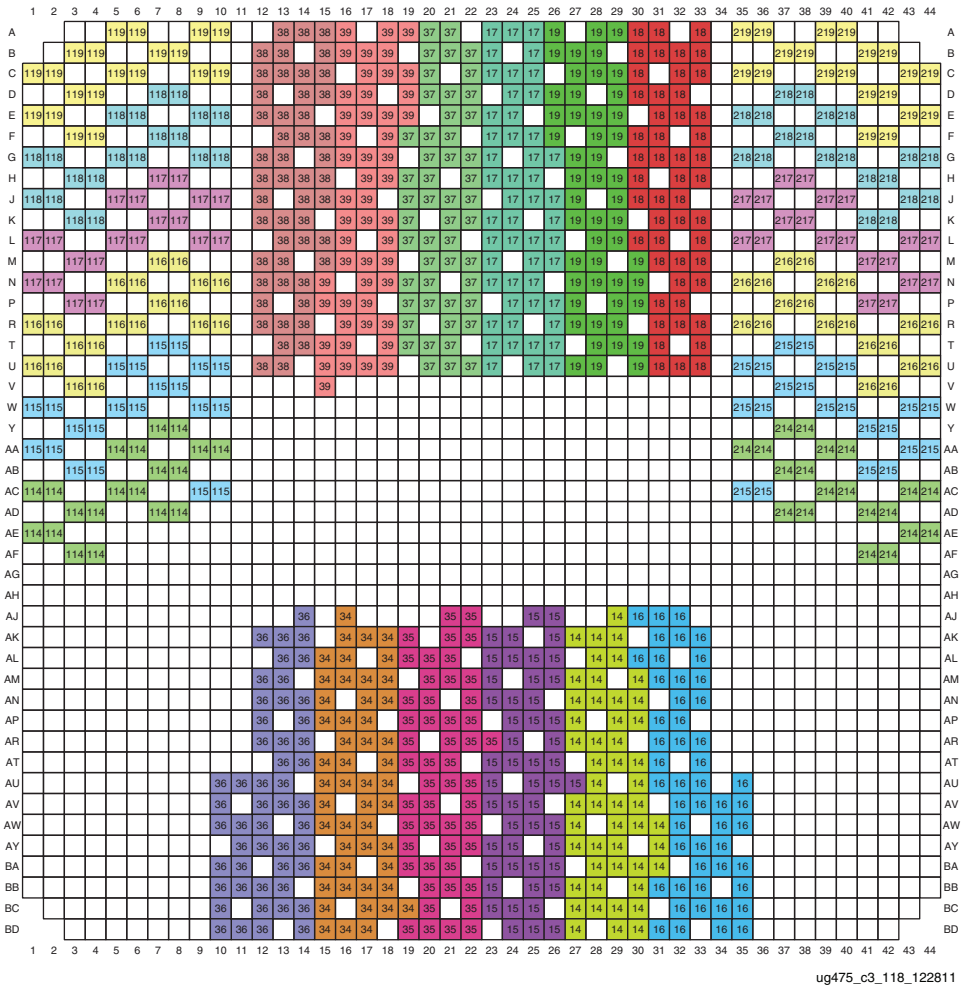


Figure 3-98: **FFG1927 Package—XC7VX415T I/O Banks**

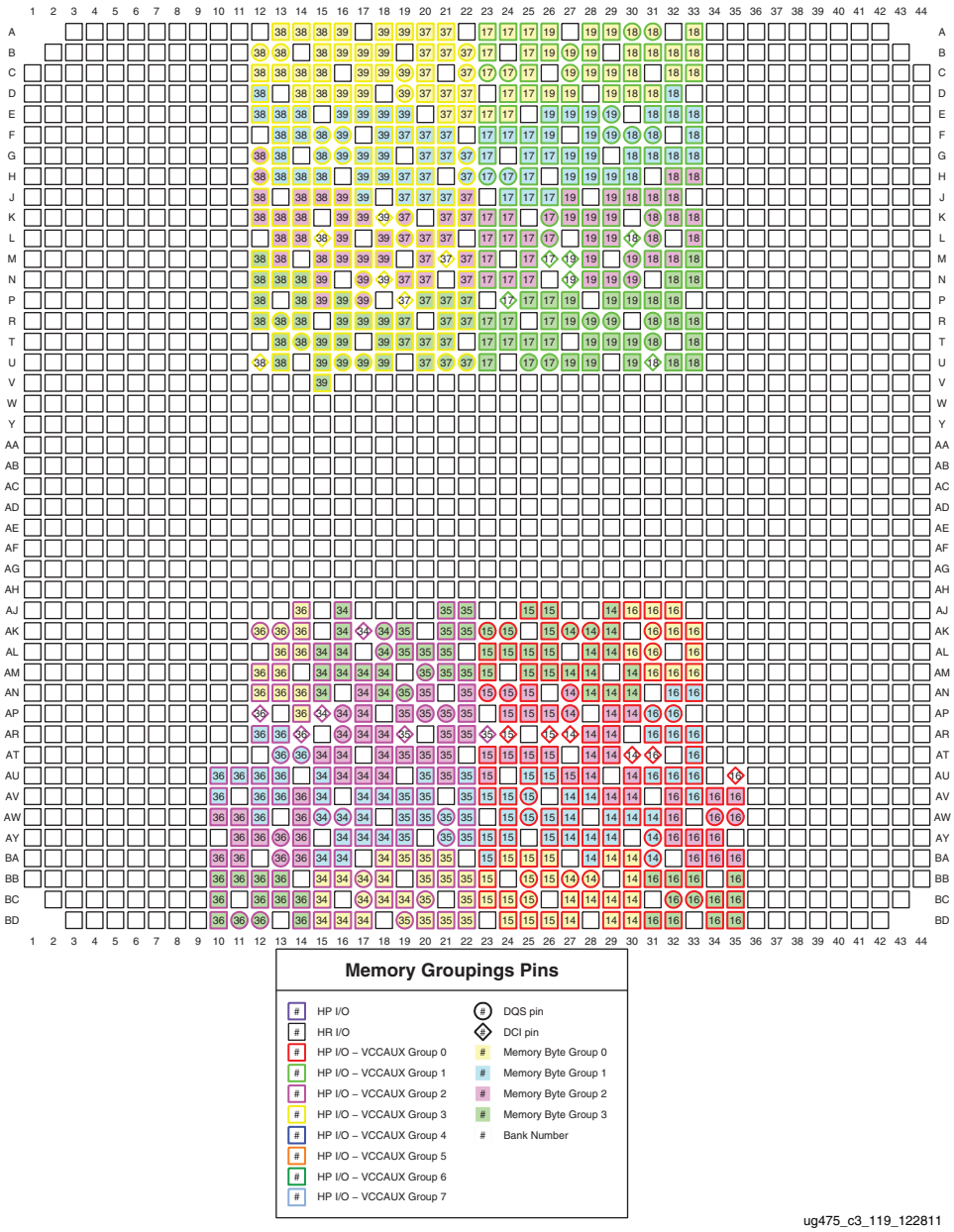


Figure 3-99: **FFG1927 Package—XC7VX415T Memory Groupings**

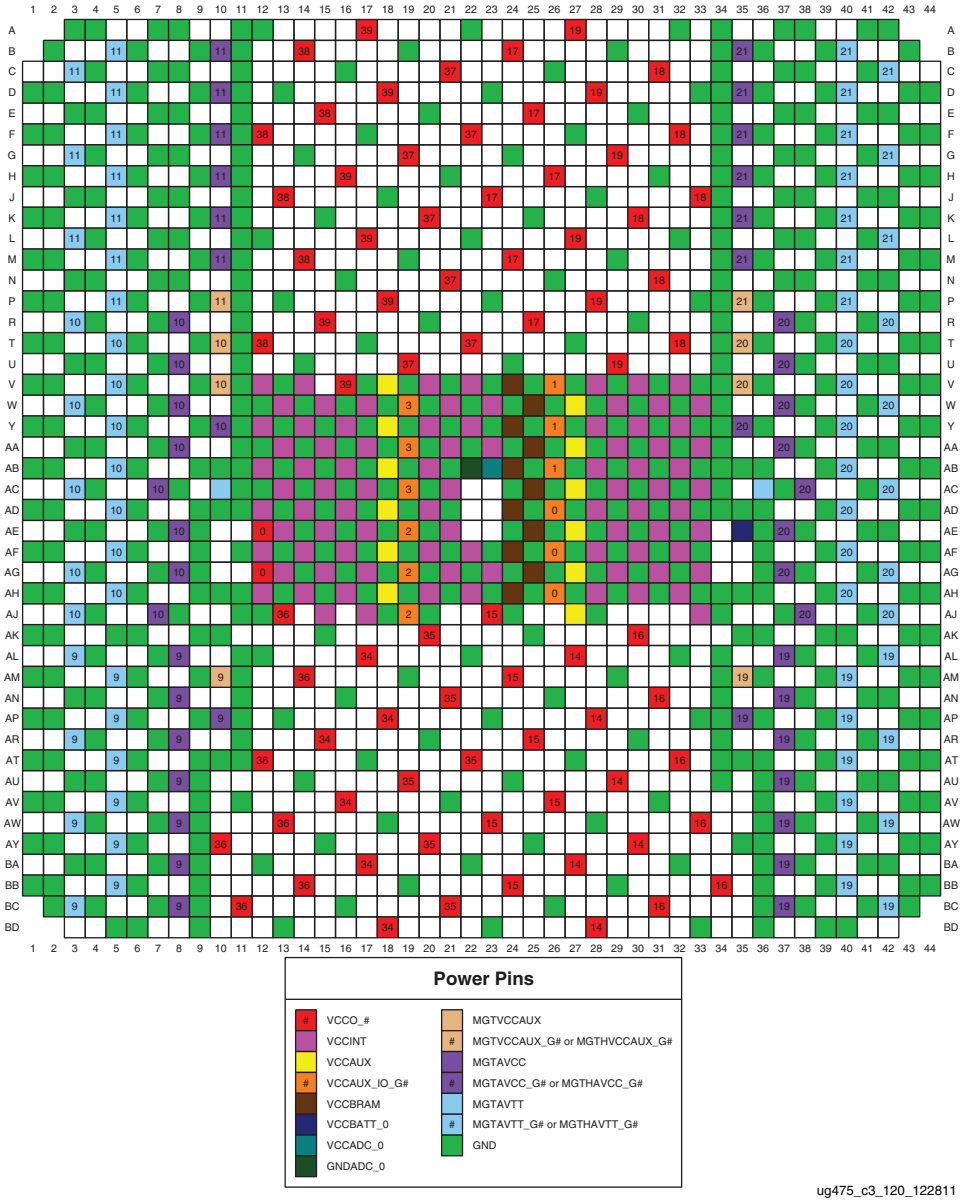


Figure 3-100: **FFG1927 Package—XC7VX415T Power and GND Placement**

FFG1157 Package—XC7VX485T

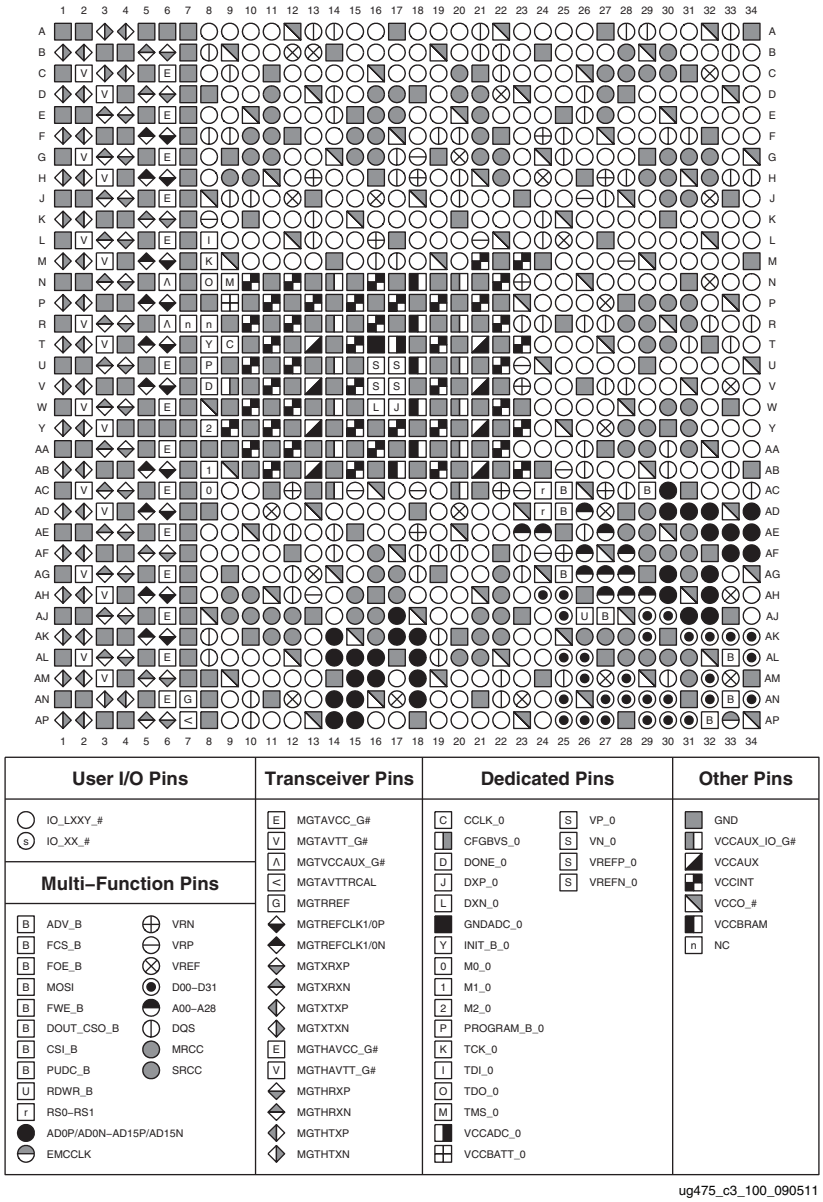


Figure 3-101: **FFG1157 Package—XC7VX485T Pinout Diagram**

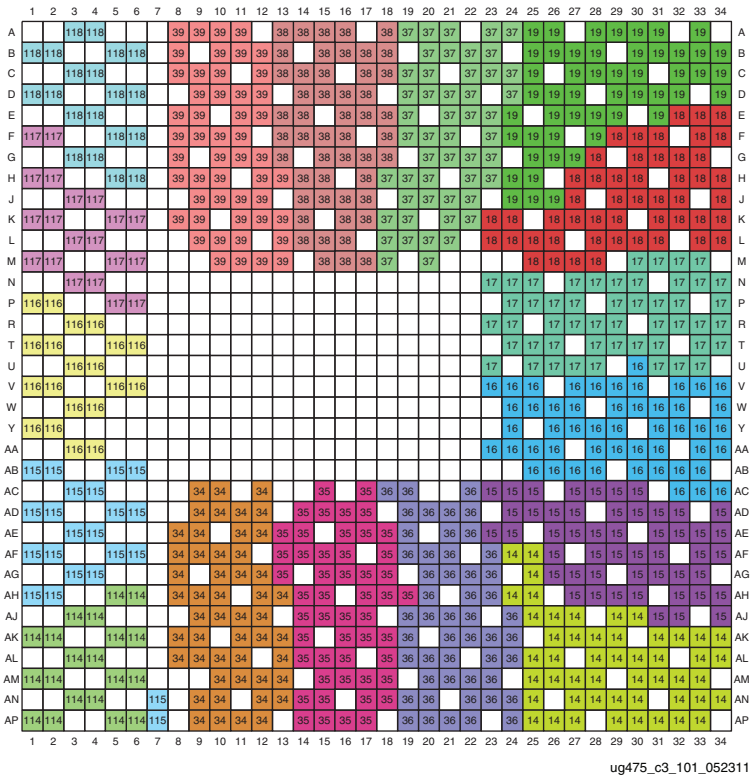


Figure 3-102: **FFG1157 Package—XC7VX485T I/O Banks**

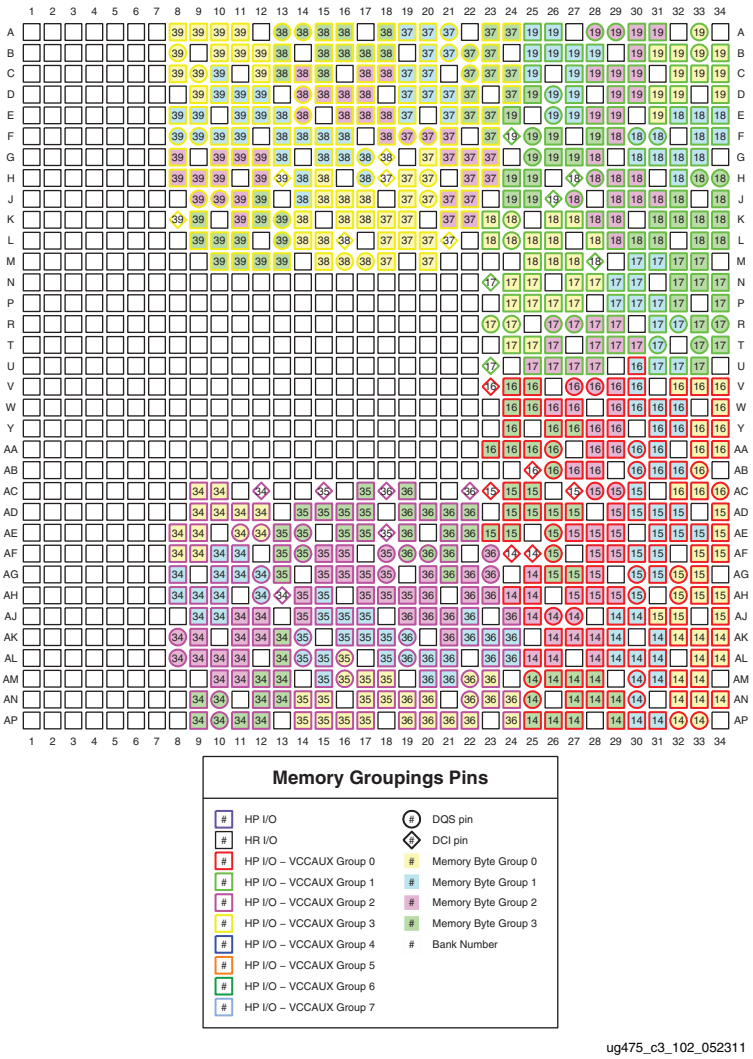


Figure 3-103: **FFG1157 Package—XC7VX485T Memory Groupings**

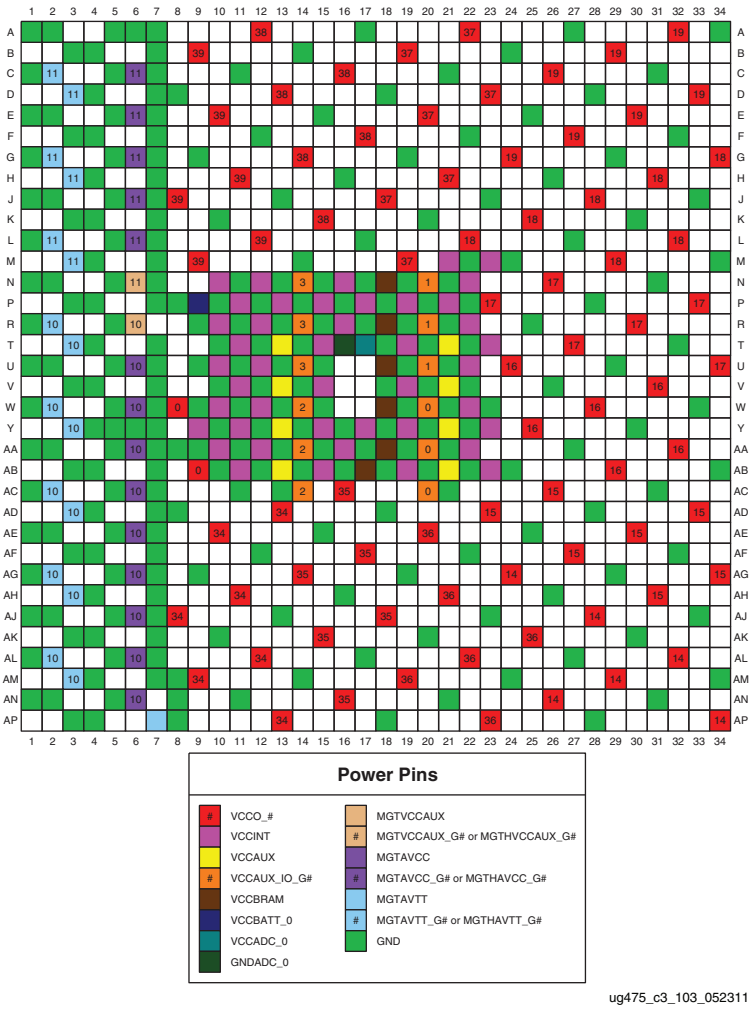
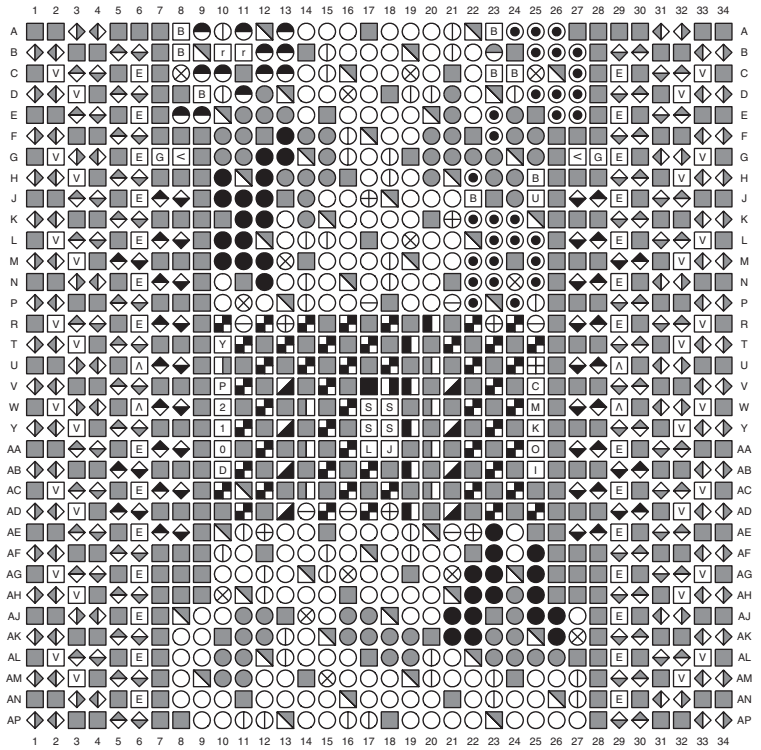


Figure 3-104: **FFG1157 Package—XC7VX485T Power and GND Placement**

FFG1158 Package—XC7VX485T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	VP_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VN_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	DONE_0	VREFP_0	VCCAUX
ADV_B	MGTAVTTRCAL	DXP_0	VREFN_0	VCCINT
FCS_B	MGTRREF	DXN_0		VCCO_#
FOE_B	MGTREFCLK1/0P	GNDADC_0		VCCBRAM
MOSI	MGTREFCLK1/0N	INIT_B_0		NC
FWE_B	MGTXRXP	M0_0		
DOUT_CSO_B	MGTXRXN	M1_0		
CSI_B	MGTXTXP	M2_0		
PUDC_B	MGTXTXN	PROGRAM_B_0		
RDWR_B	MGTHAVCC_G#	TCK_0		
RS0–RS1	MGTHAVTT_G#	TDI_0		
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0		
EMCCLK	MGTHRXN	TMS_0		
VRN	MGTHTXP	VCCADC_0		
VRP	MGTHTXN	VCCBATT_0		
VREF				
D00–D31				
A00–A28				
DQS				
MRCC				
SRCC				

ug475_c3_104_090511

Figure 3-105: **FFG1158 Package—XC7VX485T Pinout Diagram**

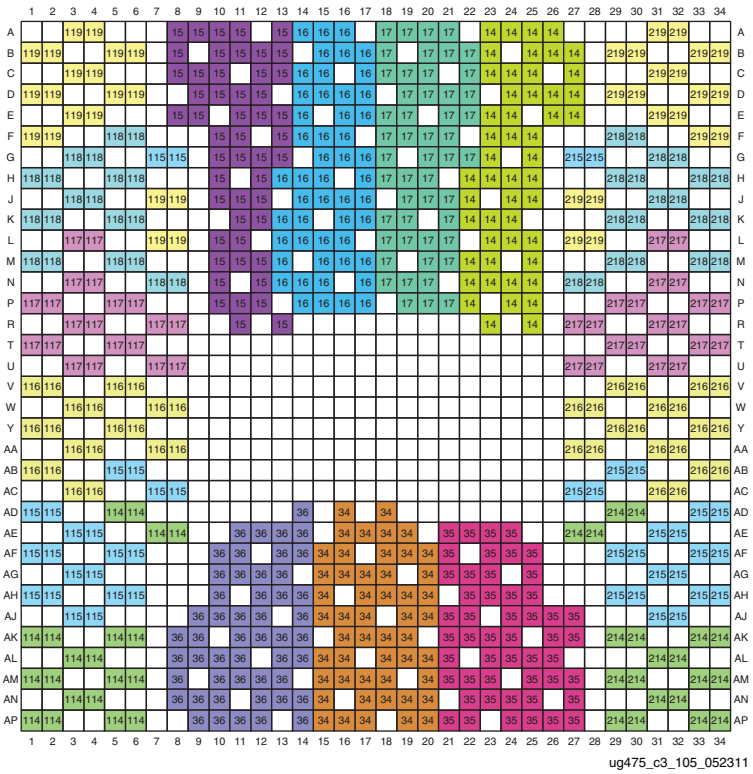


Figure 3-106: **FFG1158 Package—XC7VX485T I/O Banks**

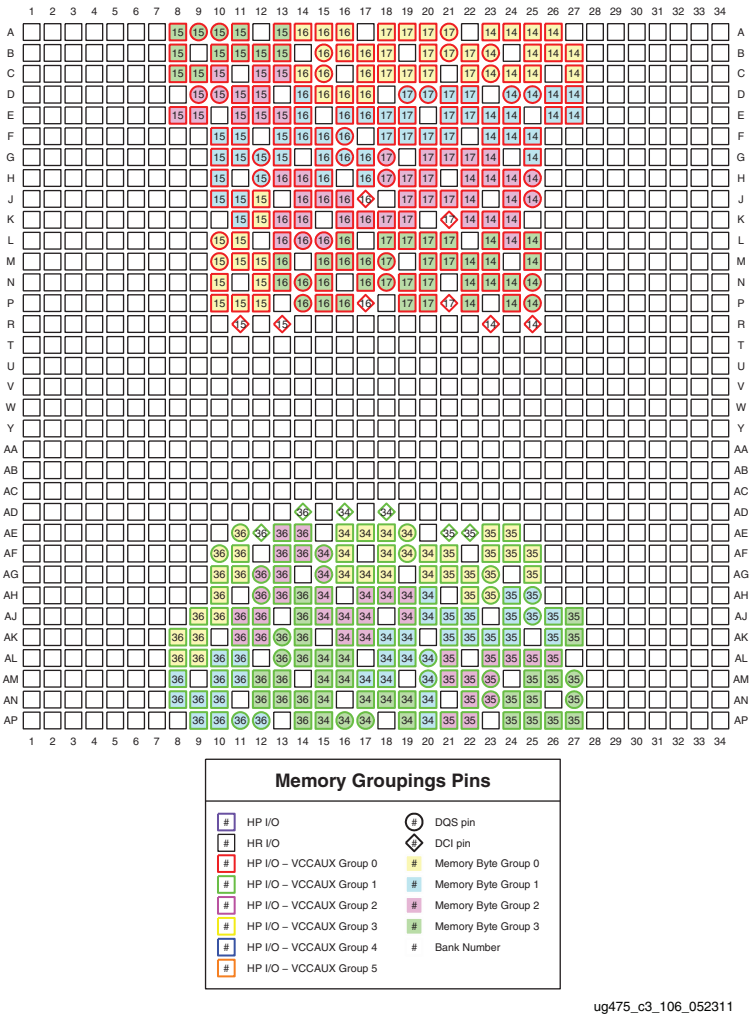


Figure 3-107: **FFG1158 Package—XC7VX485T Memory Groupings**

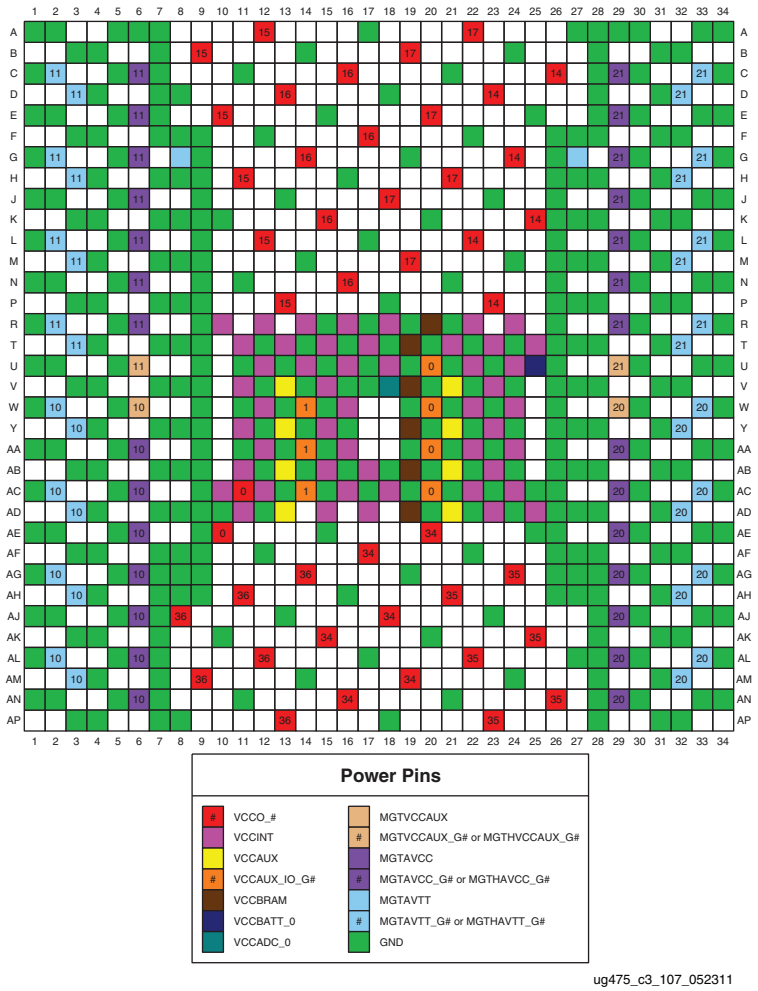


Figure 3-108: **FFG1158 Package—XC7VX485T Power and GND Placement**

FFG1761 Package—XC7VX485T

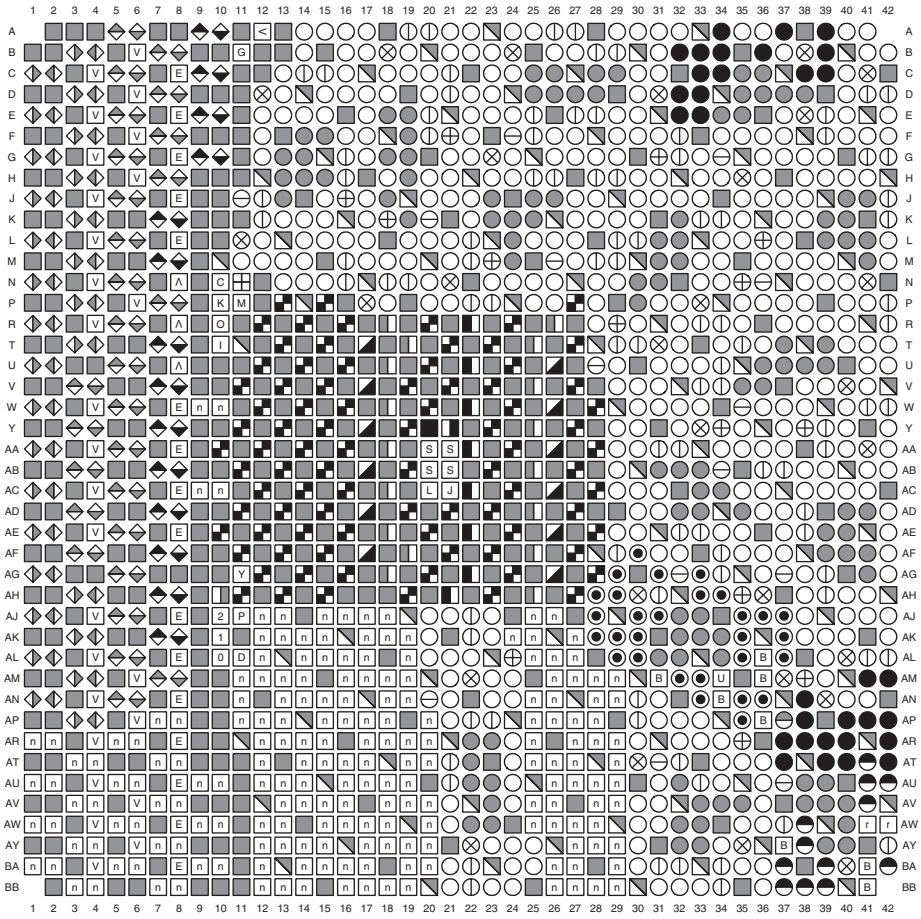


Figure 3-109: **FFG1761 Package—XC7VX485T Pinout Diagram**

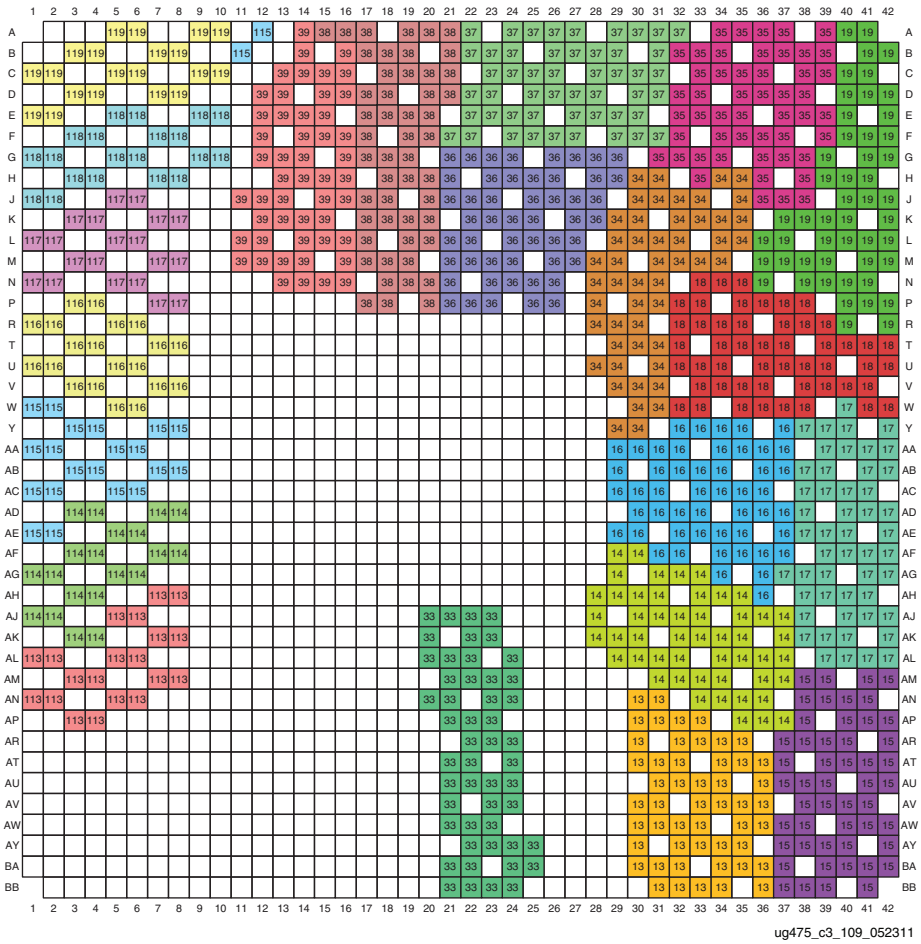


Figure 3-110: **FFG1761 Package—XC7VX485T I/O Banks**

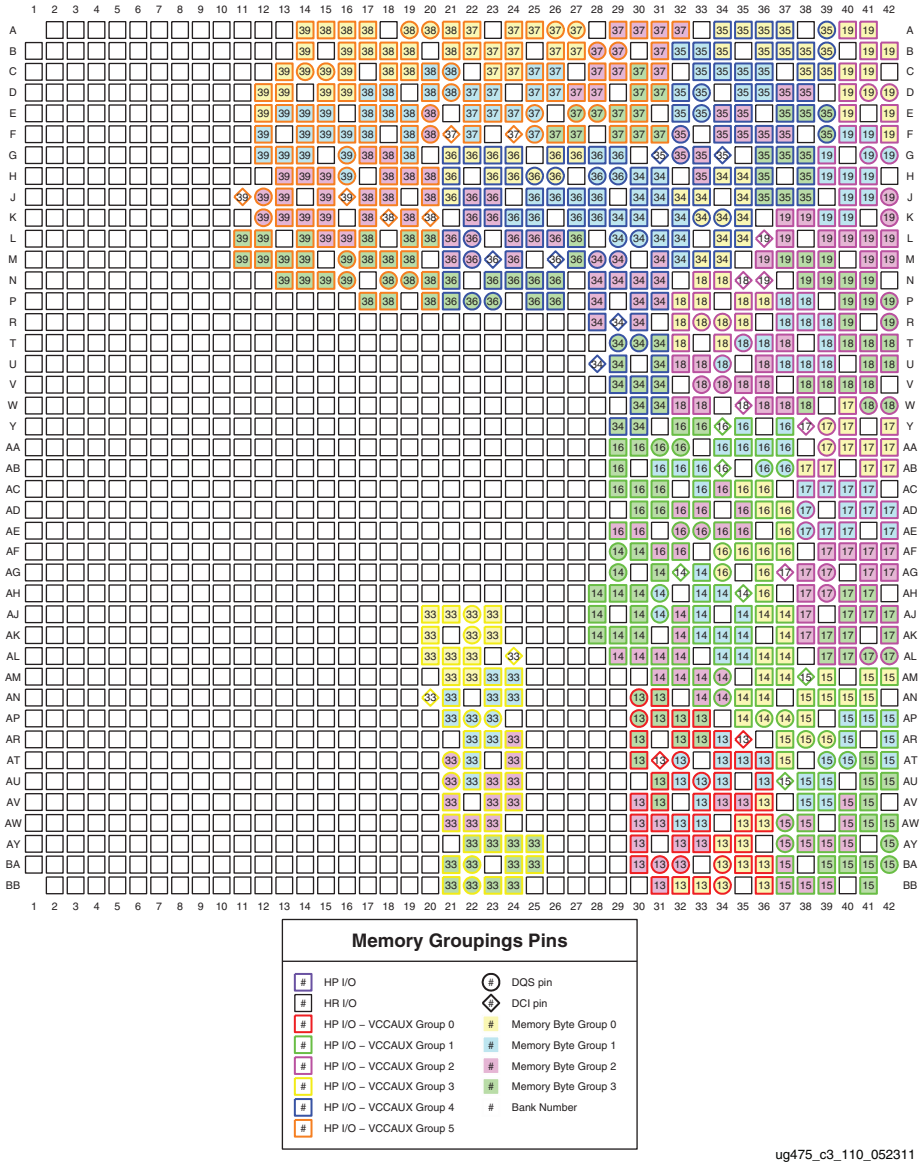


Figure 3-111: **FFG1761 Package—XC7VX485T Memory Groupings**

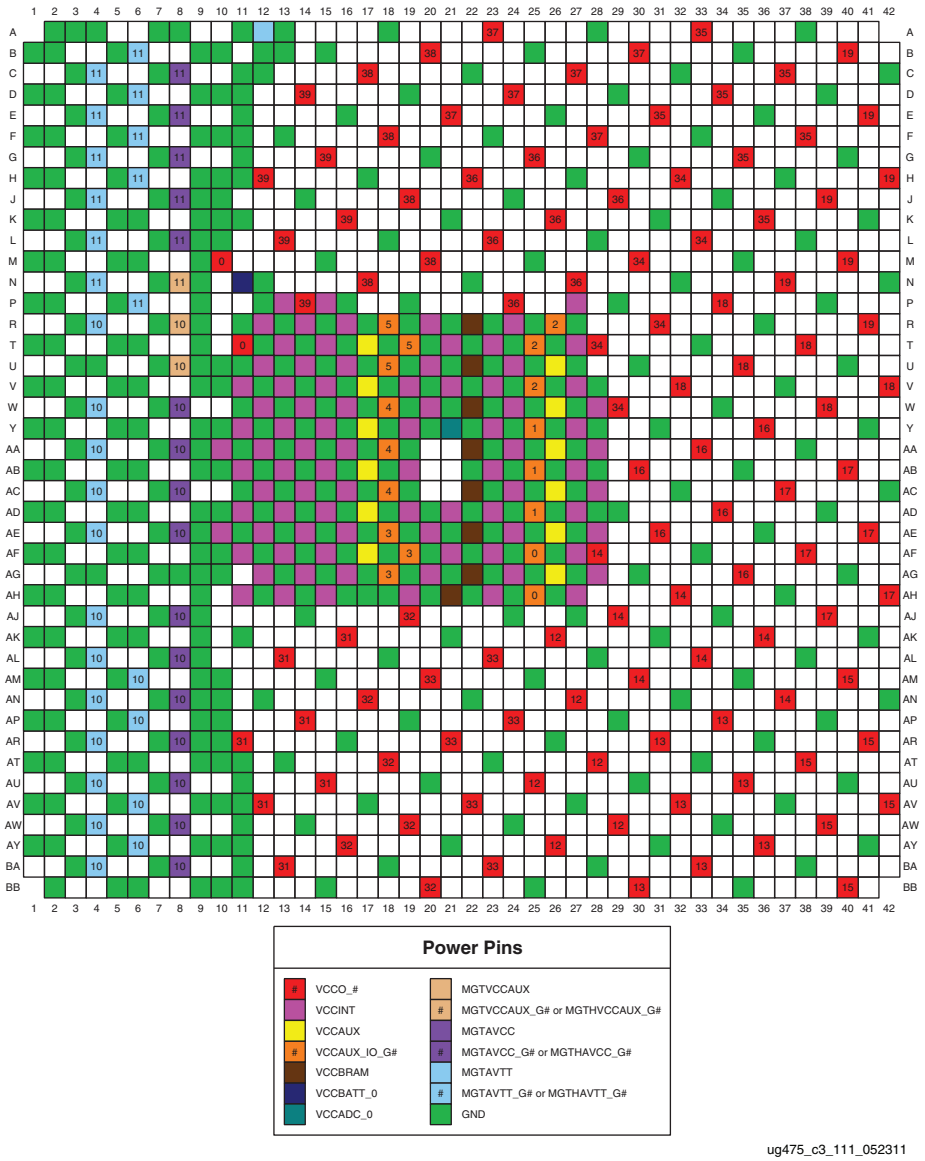


Figure 3-112: **FFG1761 Package—XC7VX485T Power and GND Placement**

FFG1927 Package—XC7VX485T

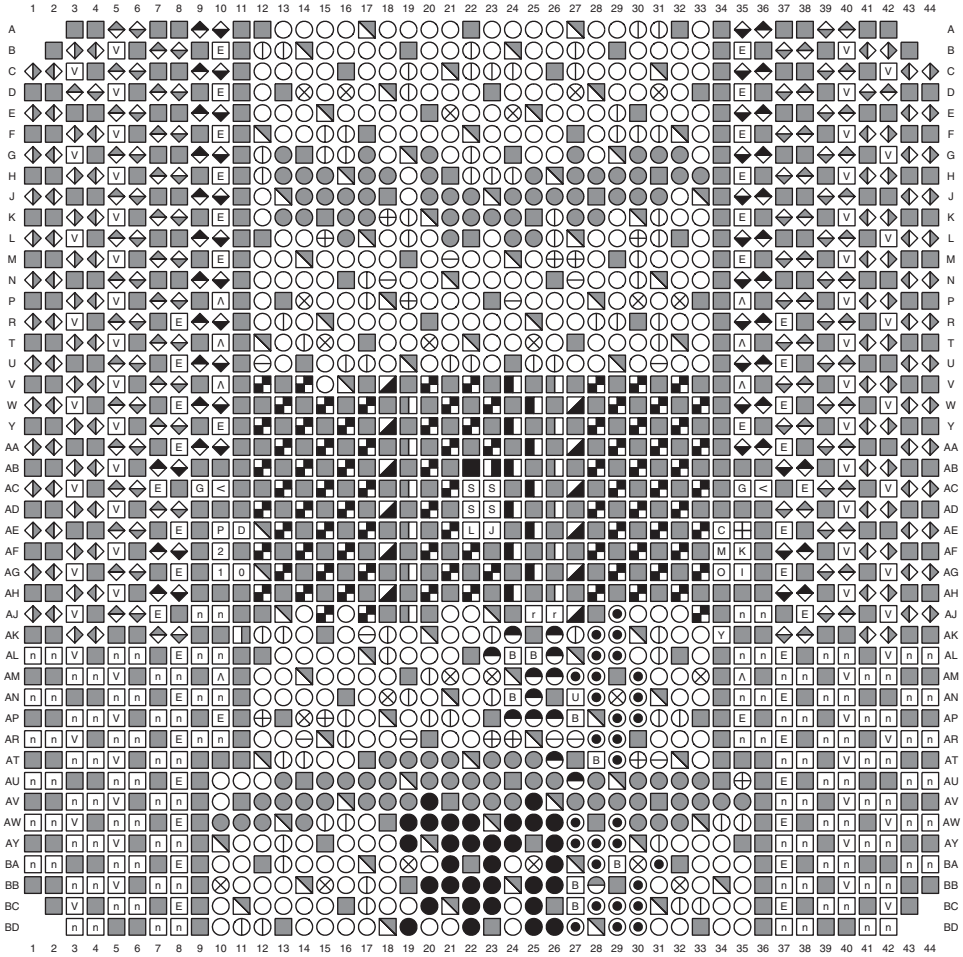


Figure 3-113: **FFG1927 Package—XC7VX485T Pinout Diagram**

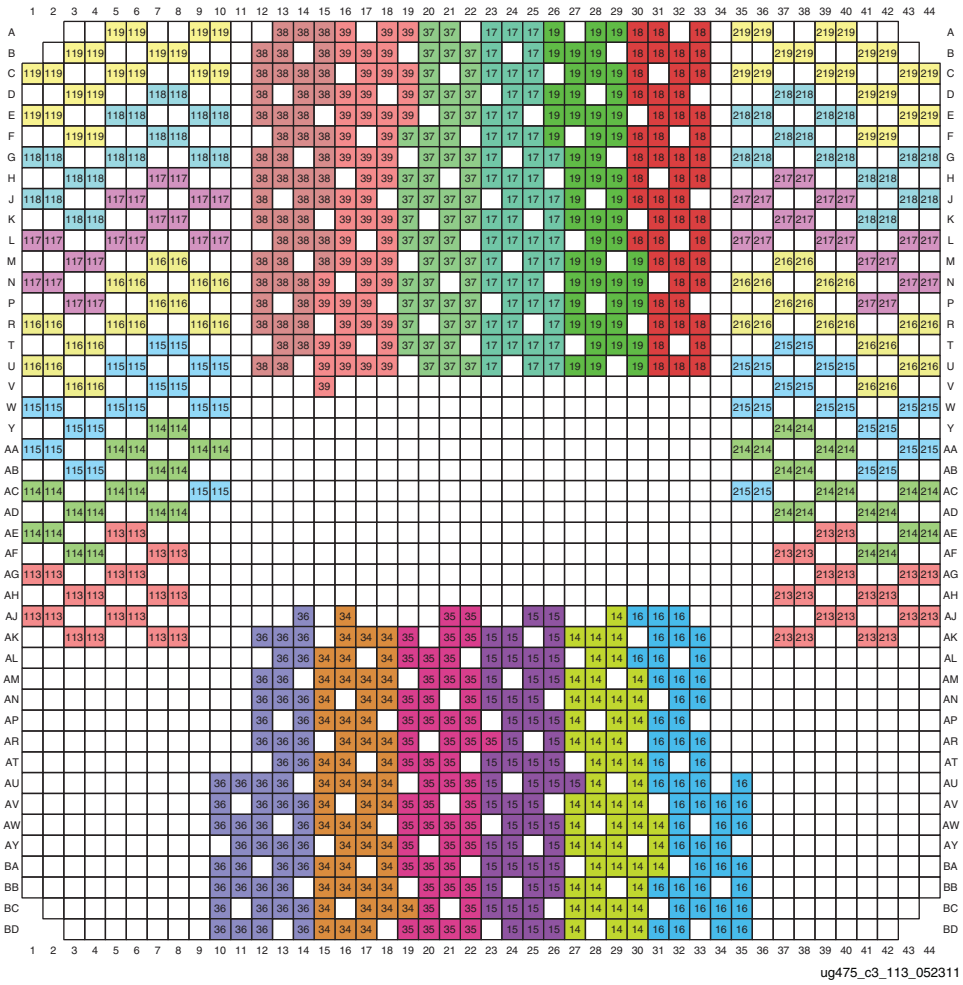


Figure 3-114: **FFG1927 Package—XC7VX485T I/O Banks**

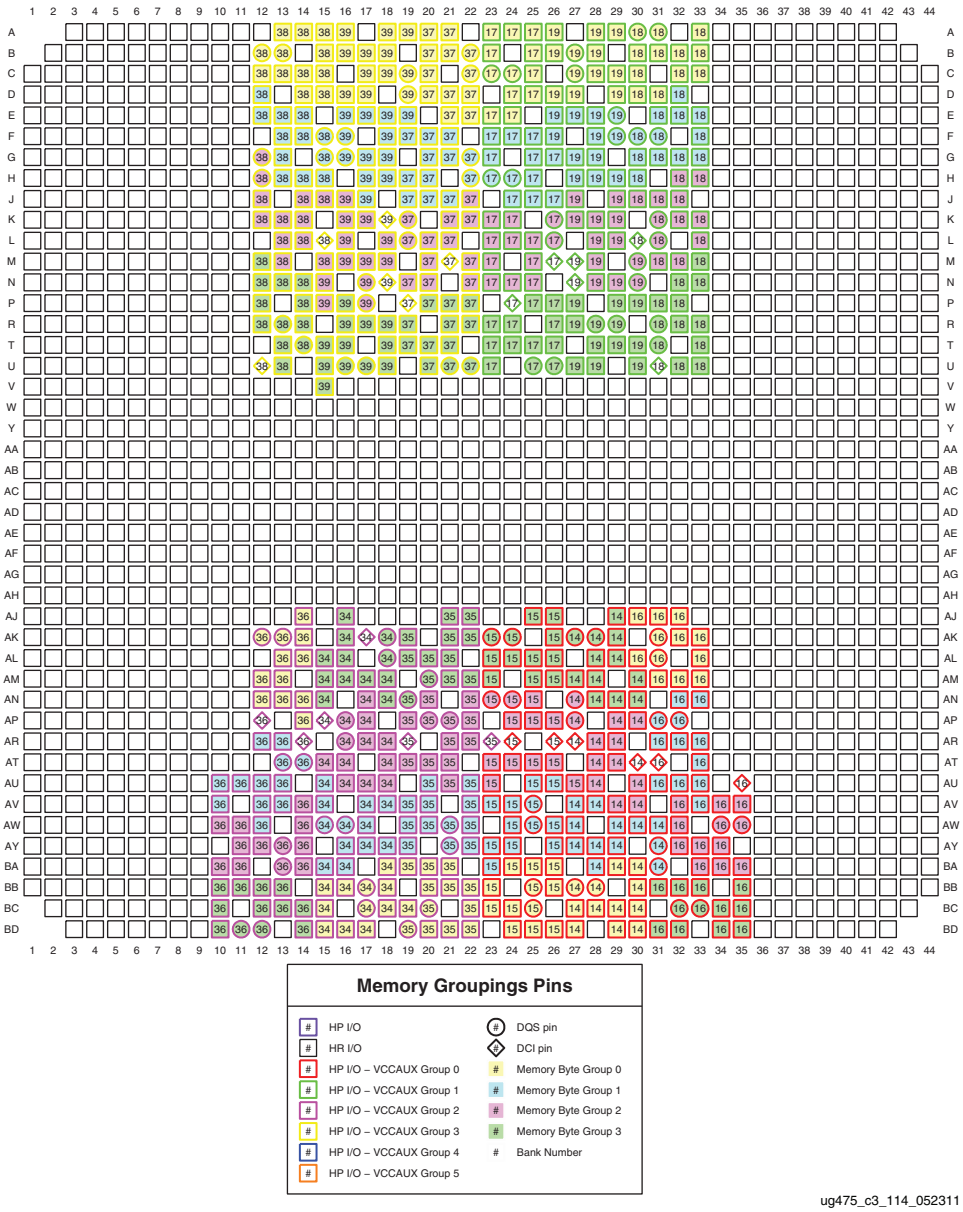


Figure 3-115: **FFG1927 Package—XC7VX485T Memory Groupings**

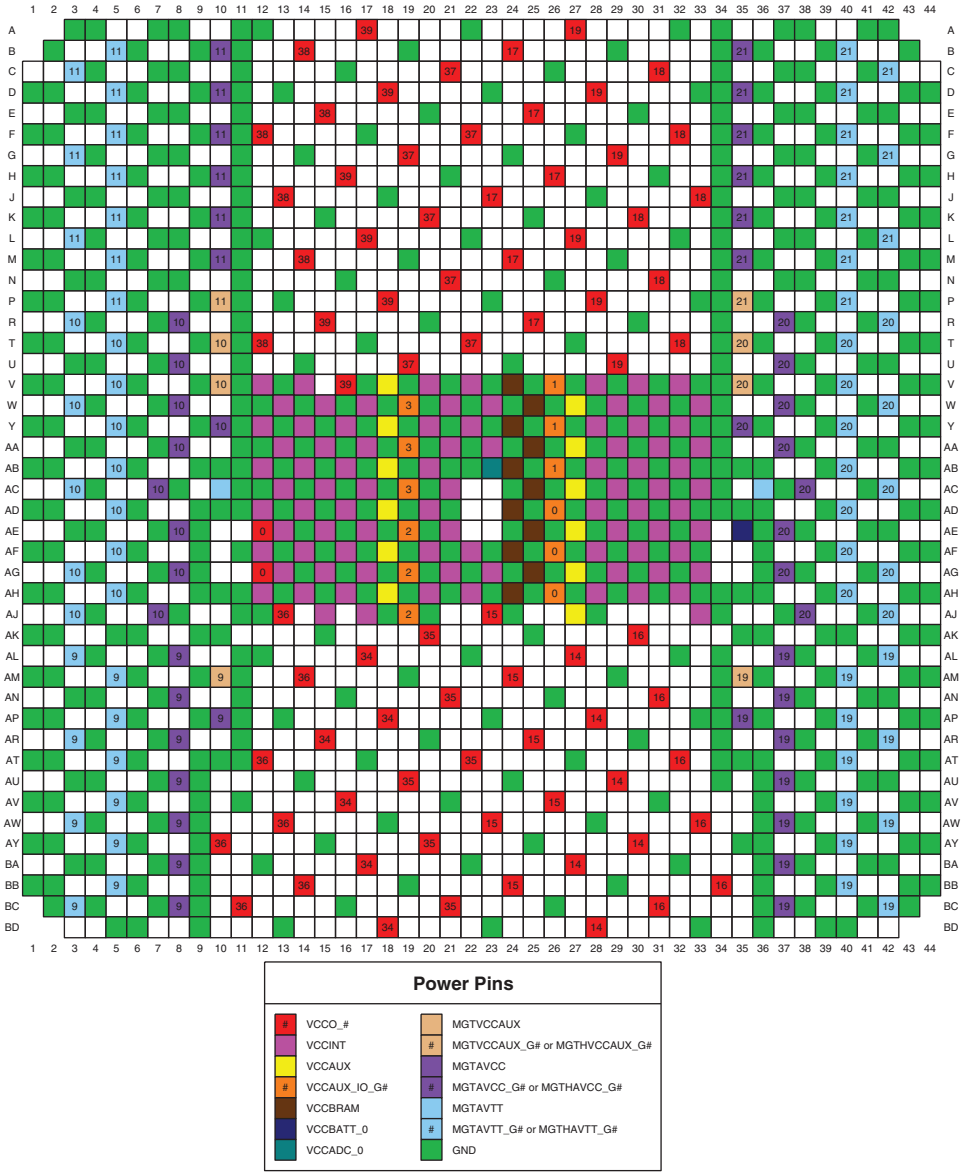


Figure 3-116: **FFG1927 Package—XC7VX485T Power and GND Placement**

FFG1930 Package—XC7VX485T

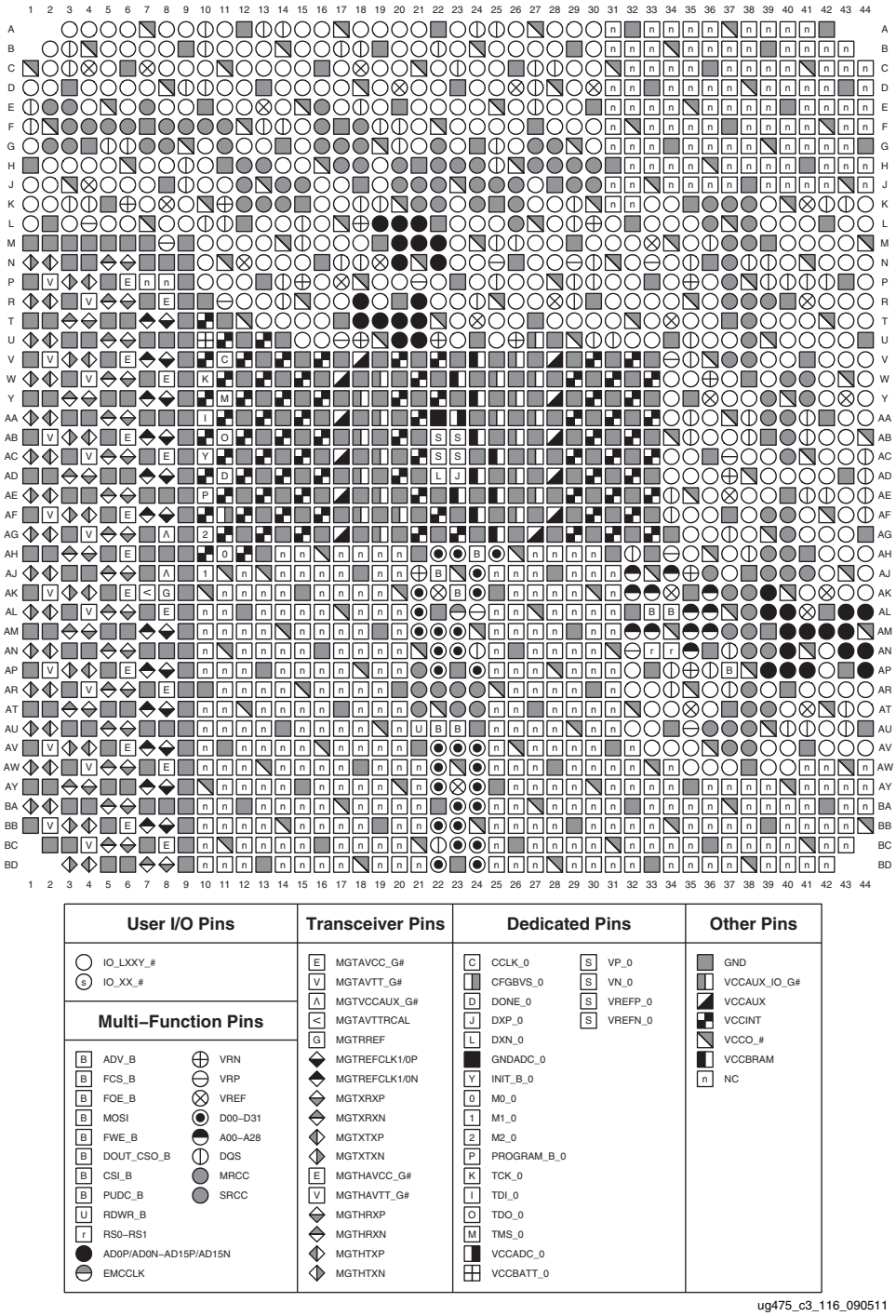


Figure 3-117: **FFG1930 Package—XC7VX485T Pinout Diagram**

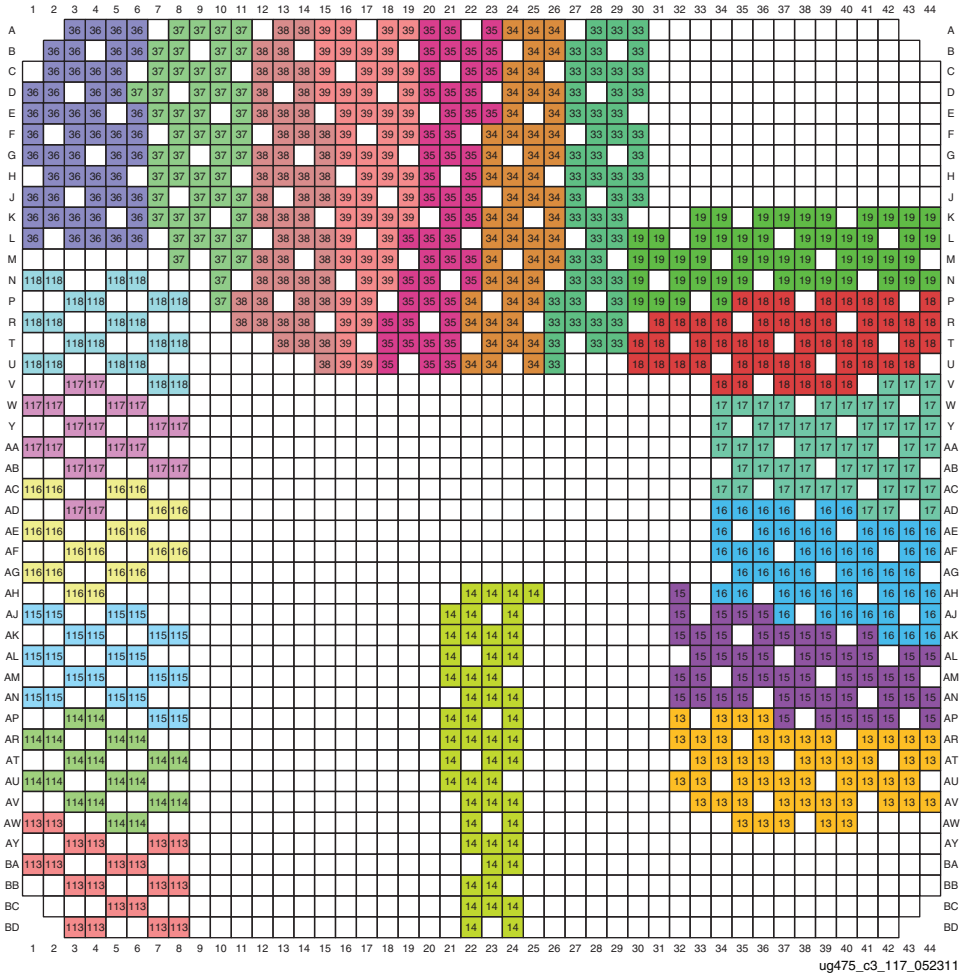


Figure 3-118: **FFG1930 Package—XC7VX485T I/O Banks**

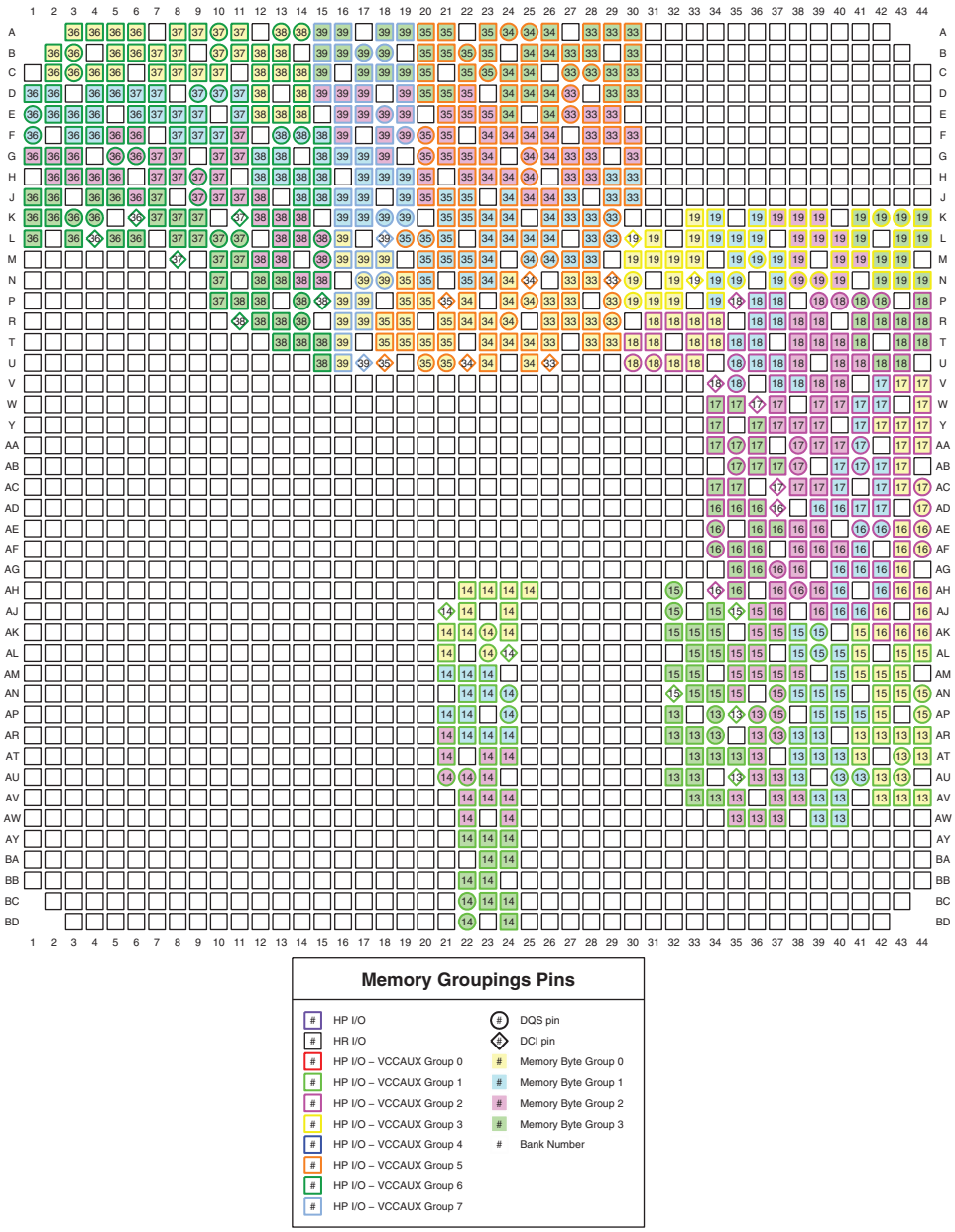


Figure 3-119: **FFG1930 Package—XC7VX485T Memory Groupings**

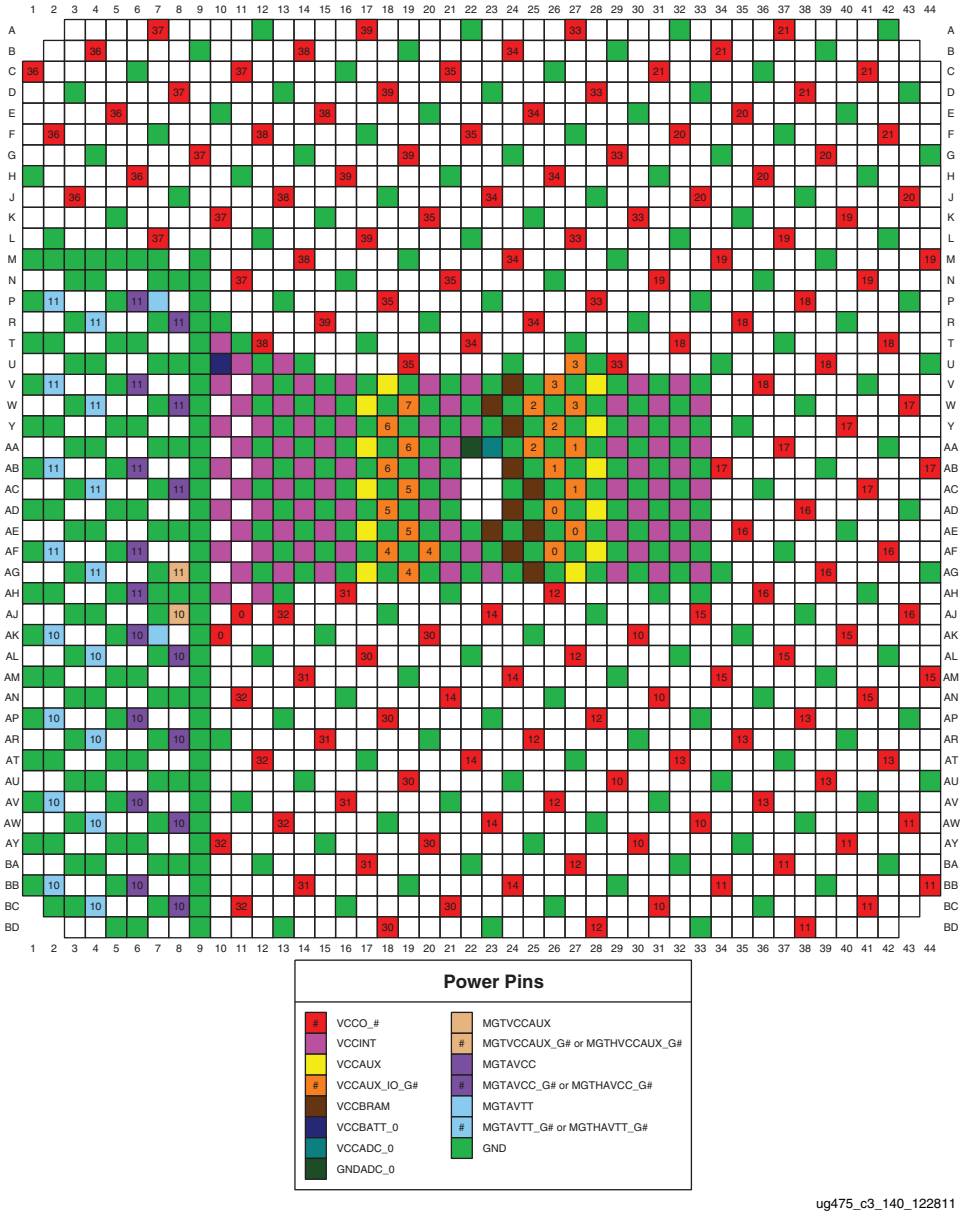


Figure 3-120: **FFG1930 Package—XC7VX485T Power and GND Placement**

FFG1761 Package—XC7VX690T

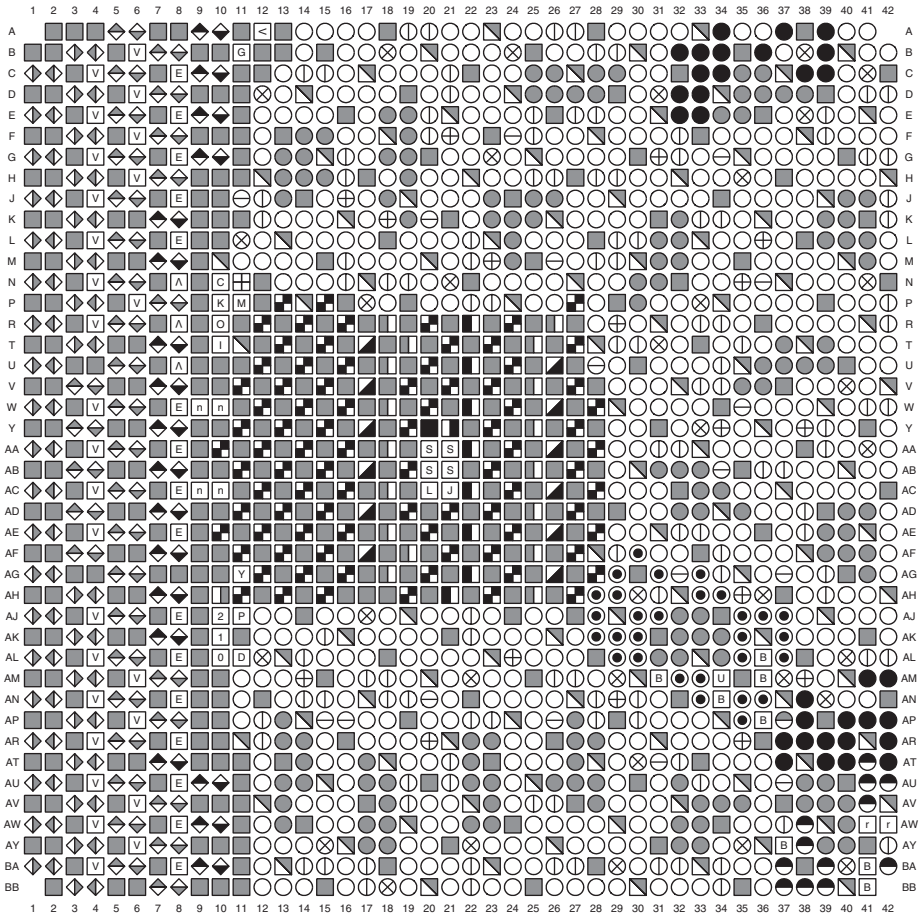


Figure 3-121: **FFG1761 Package—XC7VX690T Pinout Diagram**

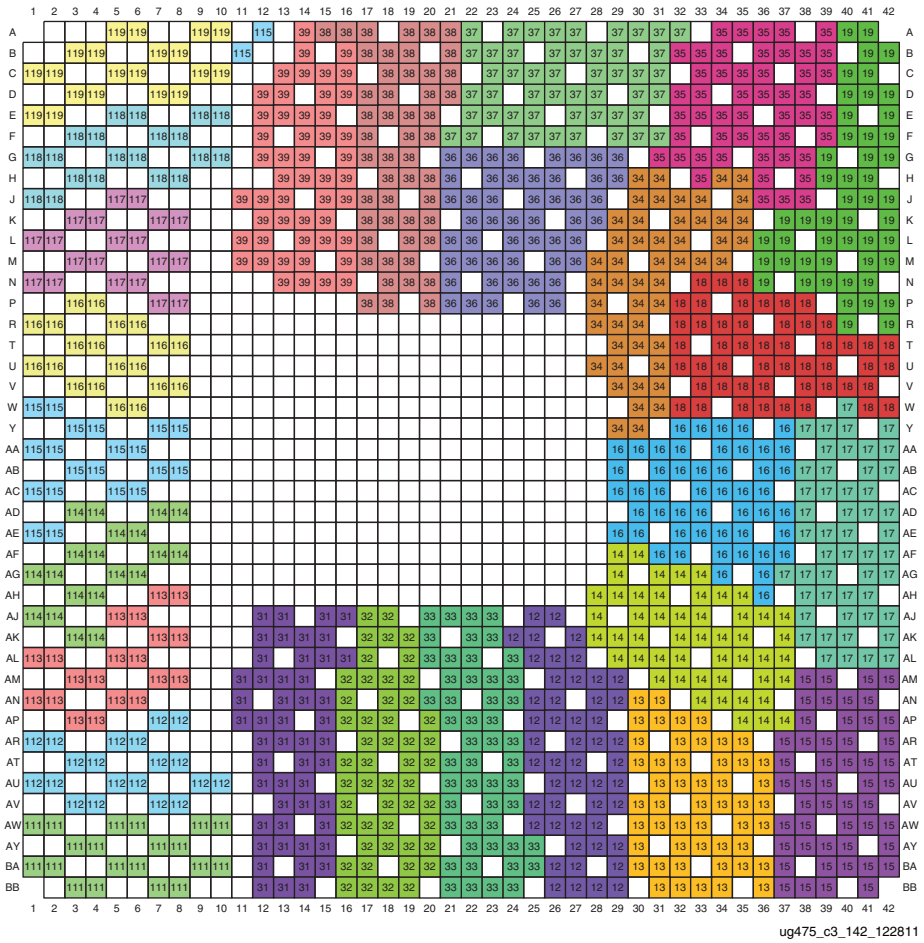


Figure 3-122: **FFG1761 Package—XC7VX690T I/O Banks**

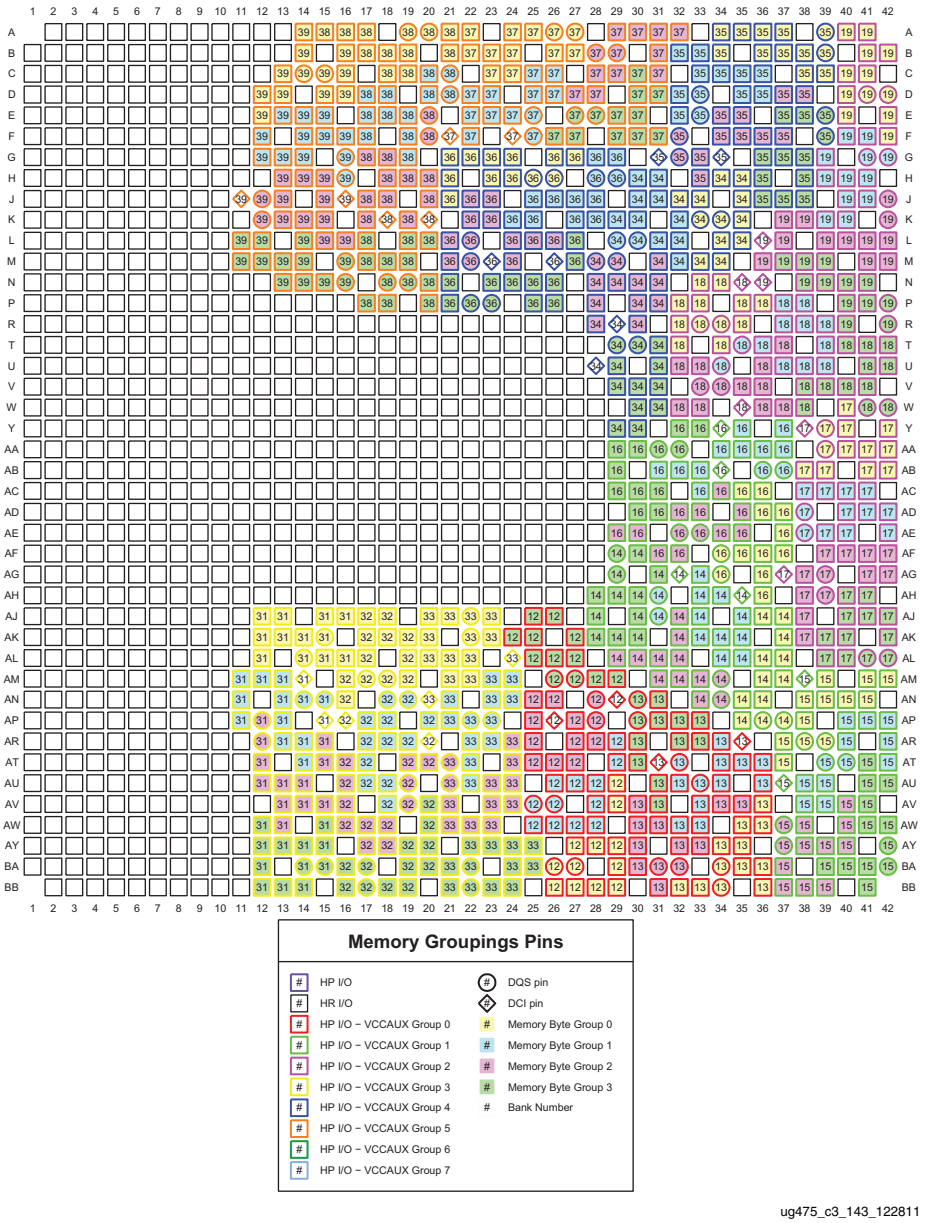


Figure 3-123: **FFG1761 Package—XC7VX690T Memory Groupings**

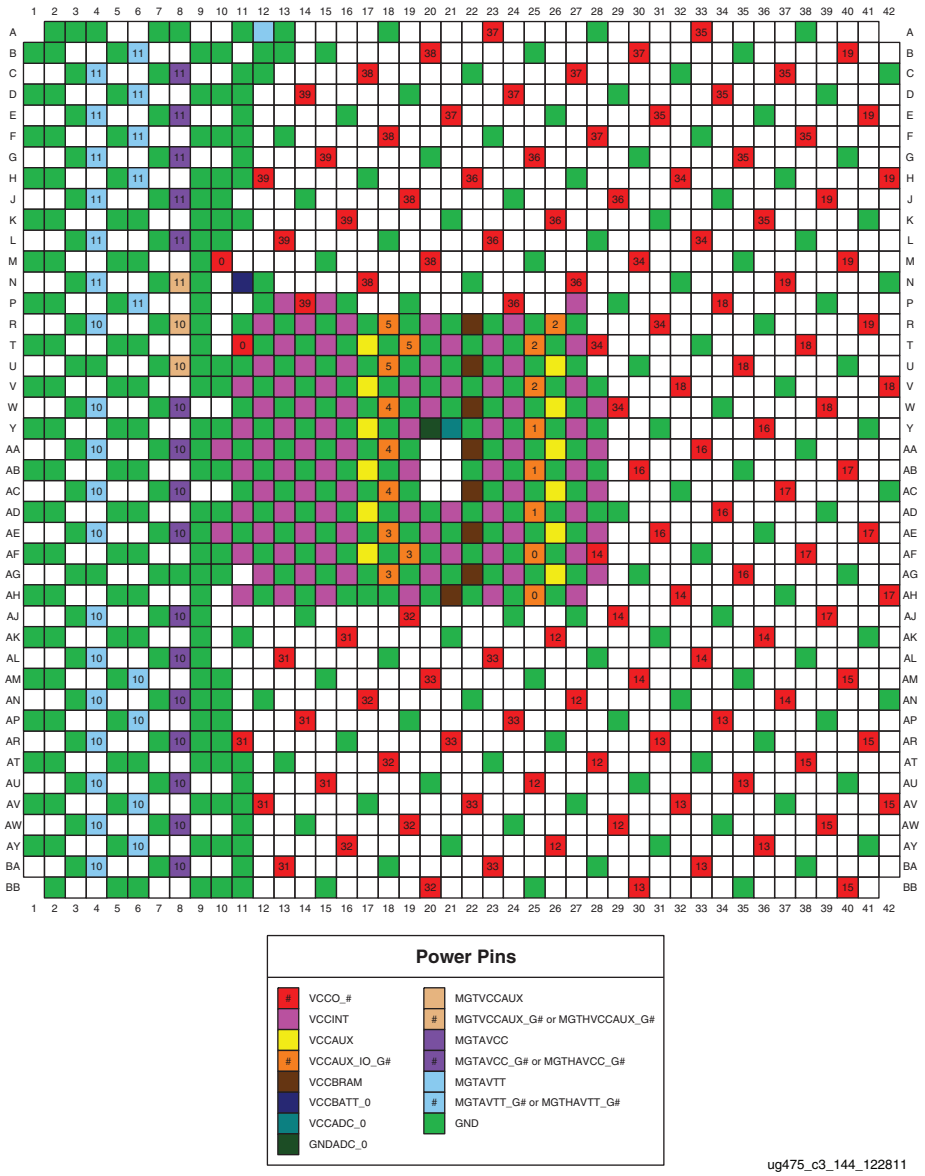
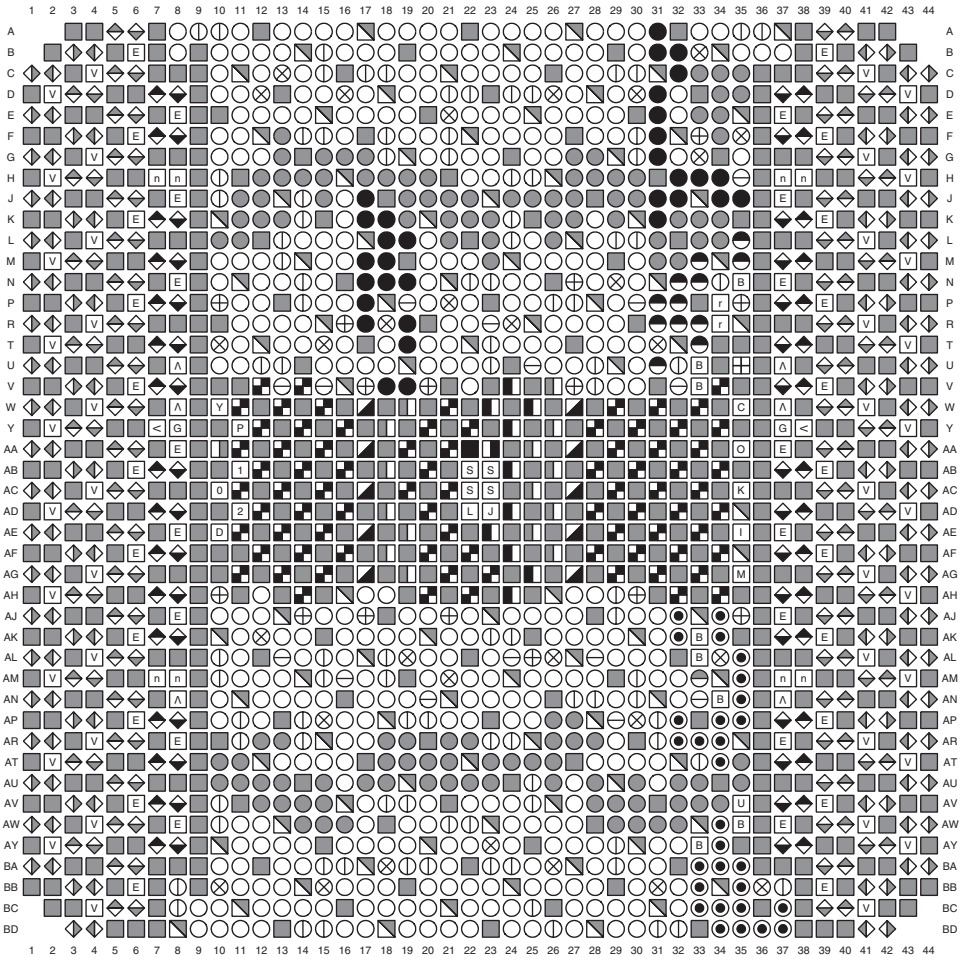


Figure 3-124: **FFG1761 Package—XC7VX690T Power and GND Placement**

FFG1926 Package—XC7VX690T and XC7VX980T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	DONE_0	VCCAUX
ADV_B	MGTAVTTRCAL	DXP_0	VCCINT
FCS_B	MGTRREF	DXN_0	VCCO_#
FOE_B	MGTREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	MGTREFCLK1/0N	INIT_B_0	NC
FWE_B	MGTXRXP	M0_0	
DOUT_CSO_B	MGTXRXN	M1_0	
CSI_B	MGTXTXP	M2_0	
PUDC_B	MGTXTXN	PROGRAM_B_0	
RDWR_B	MGTHAVCC_G#	TCK_0	
RS0–RS1	MGTHAVTT_G#	TDI_0	
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0	
EMCCLK	MGTHRXN	TMS_0	
VRN	MGTHTXP	VCCADC_0	
VRP	MGTHTXN	VCCBATT_0	
VREF		VP_0	
D00–D31		VN_0	
A00–A28		VREFP_0	
DQS		VREFN_0	
MRCC			
SRCC			

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Figure 3-125: **FFG1926 Package—XC7VX690T and XC7VX980T Pinout Diagram**

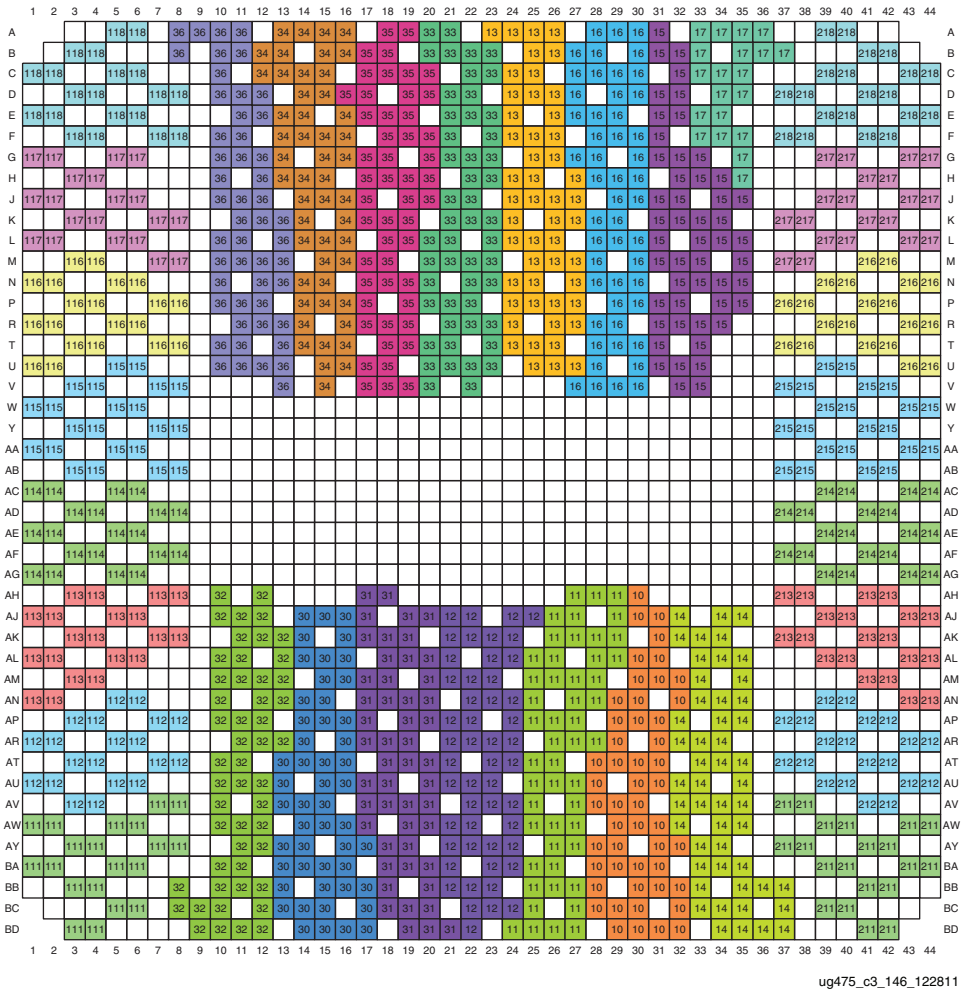


Figure 3-126: **FFG1926 Package—XC7VX690T and XC7VX980T I/O Banks**

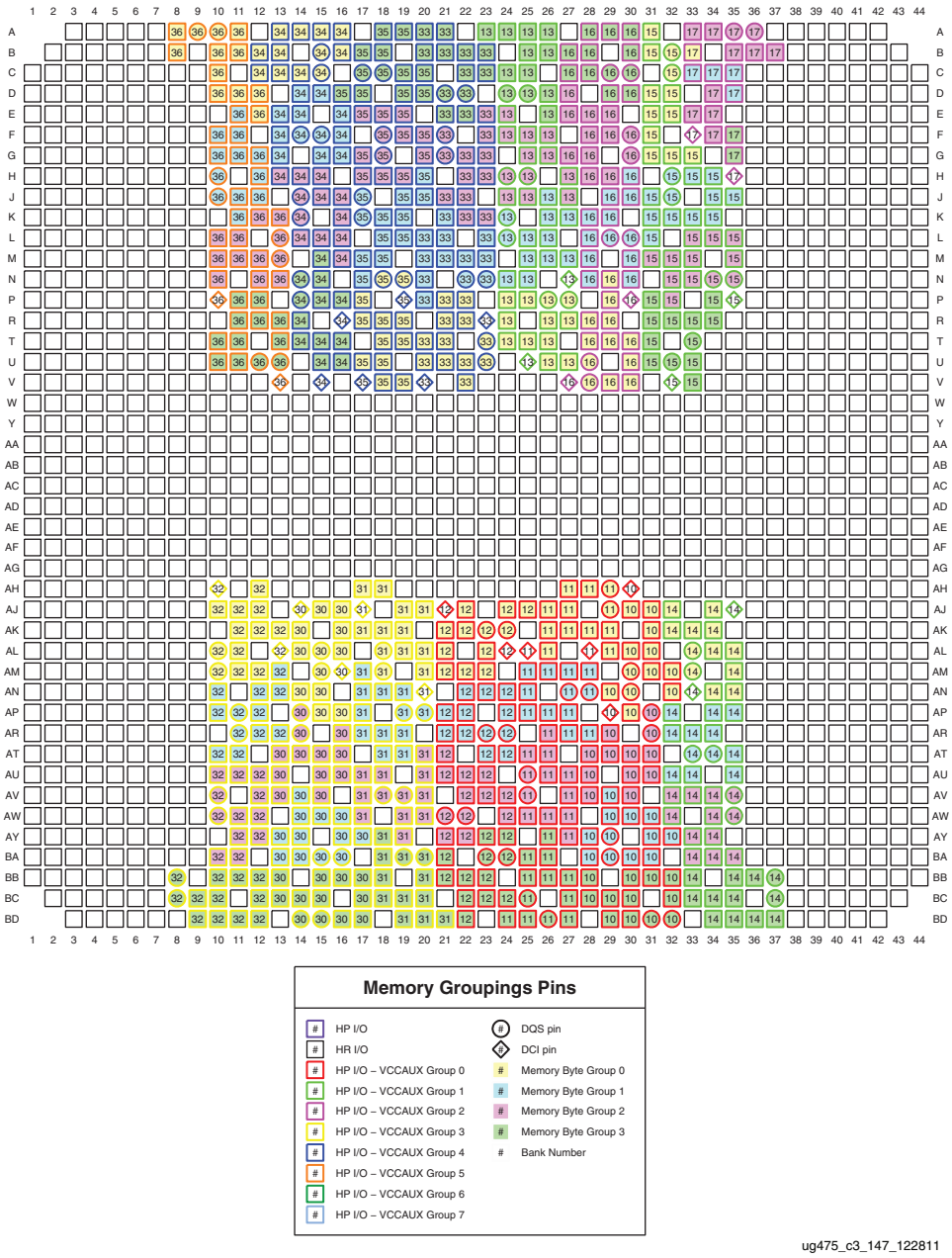


Figure 3-127: **FFG1926 Package—XC7VX690T and XC7VX980T Memory Groupings**

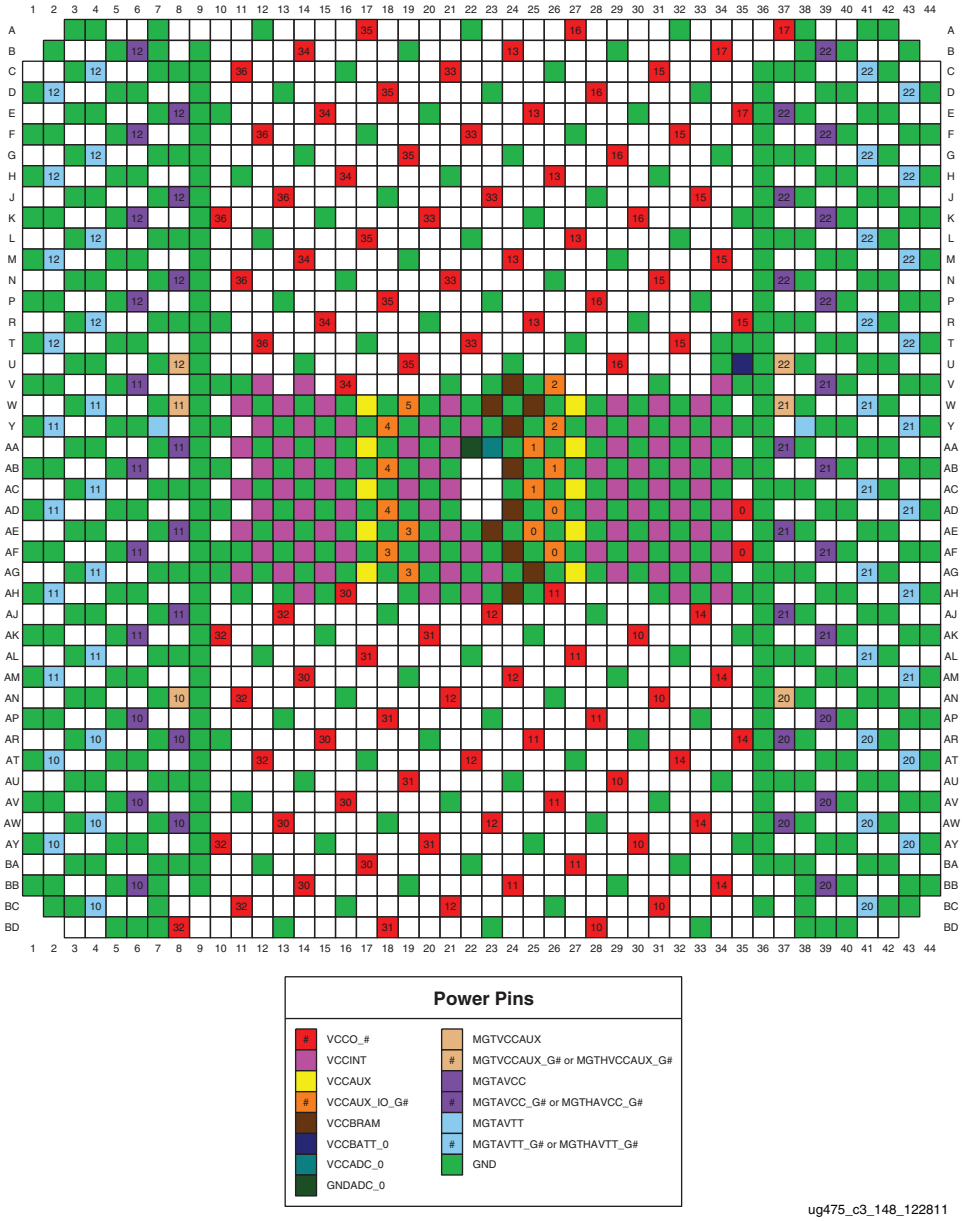


Figure 3-128: **FFG1926 Package—XC7VX690T and XC7VX980T Power and GND Placement**

FFG1927 Package—XC7VX550T and XC7VX690T

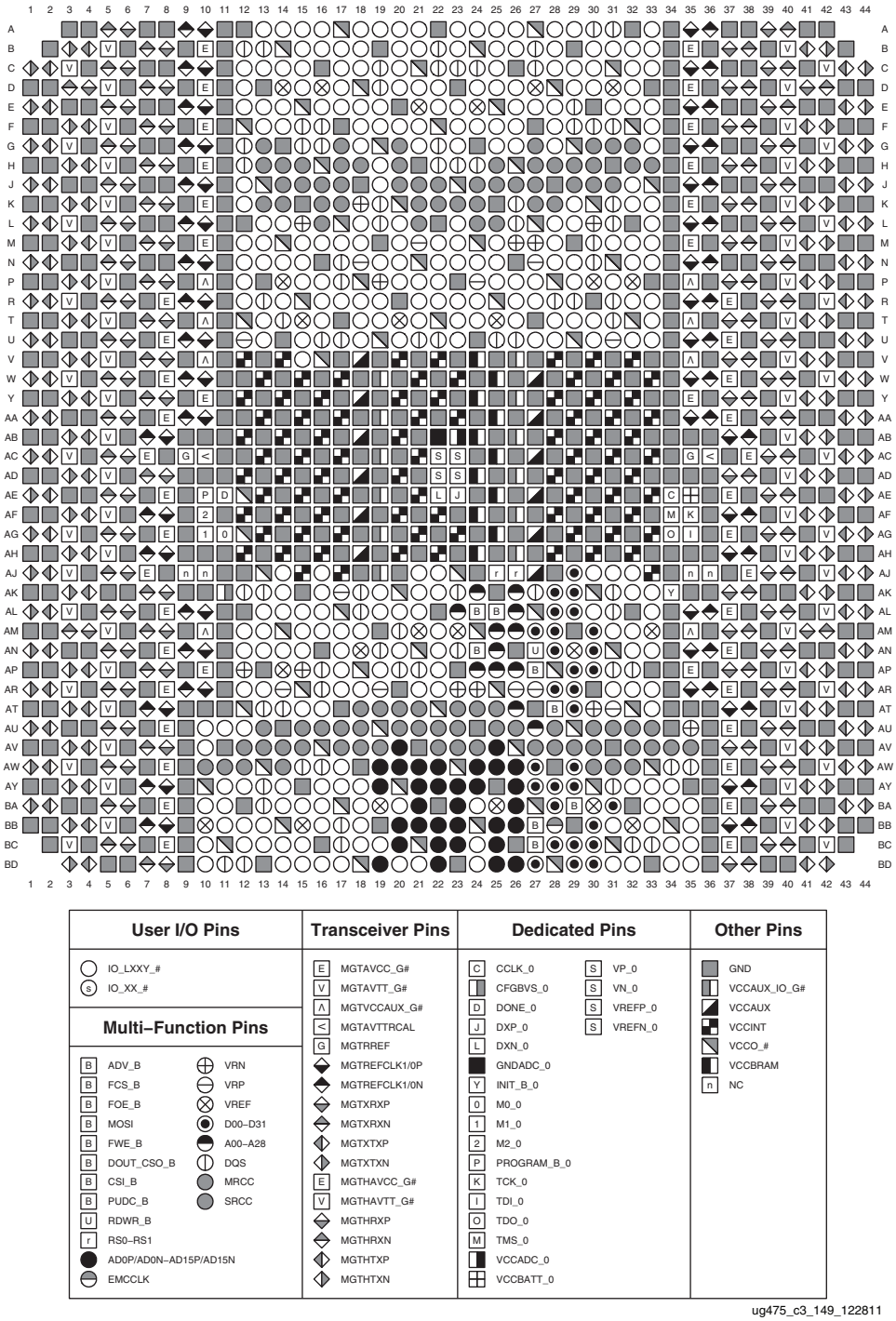


Figure 3-129: **FFG1927 Package—XC7VX550T and XC7VX690T Pinout Diagram**

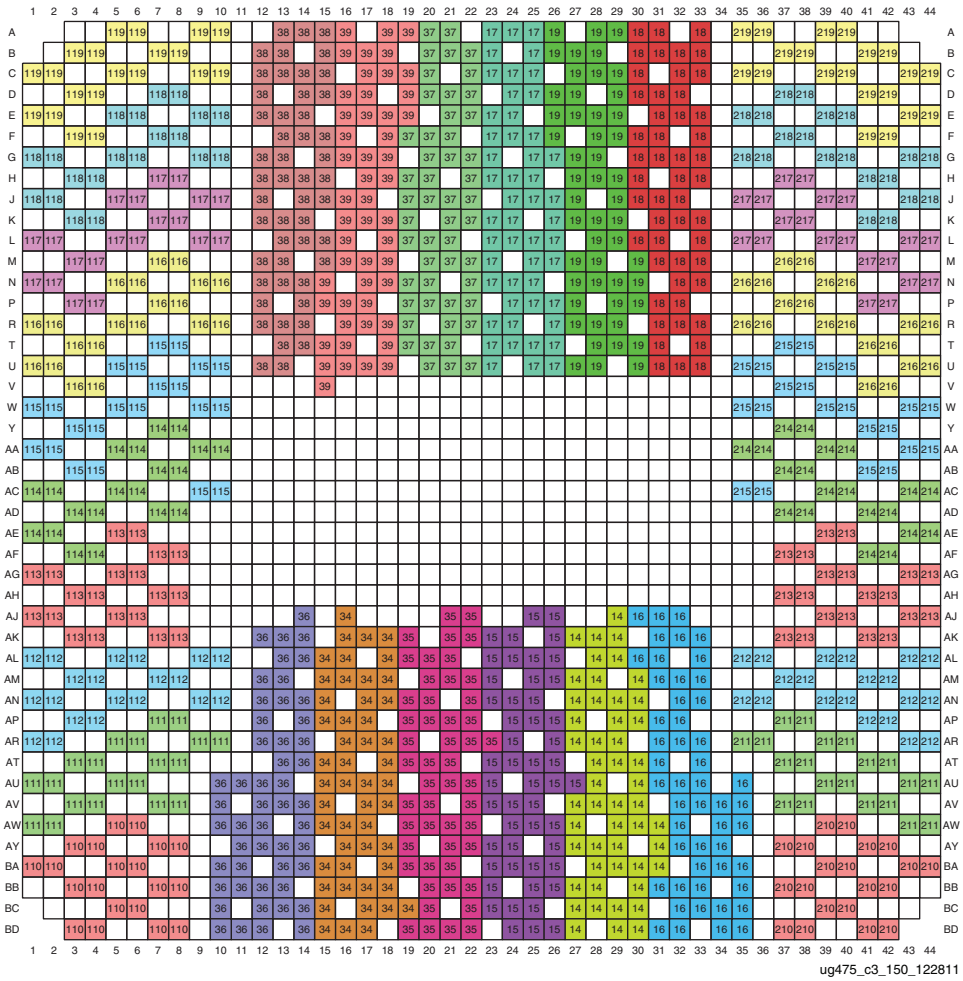


Figure 3-130: **FFG1927 Package—XC7VX550T and XC7VX690T I/O Banks**

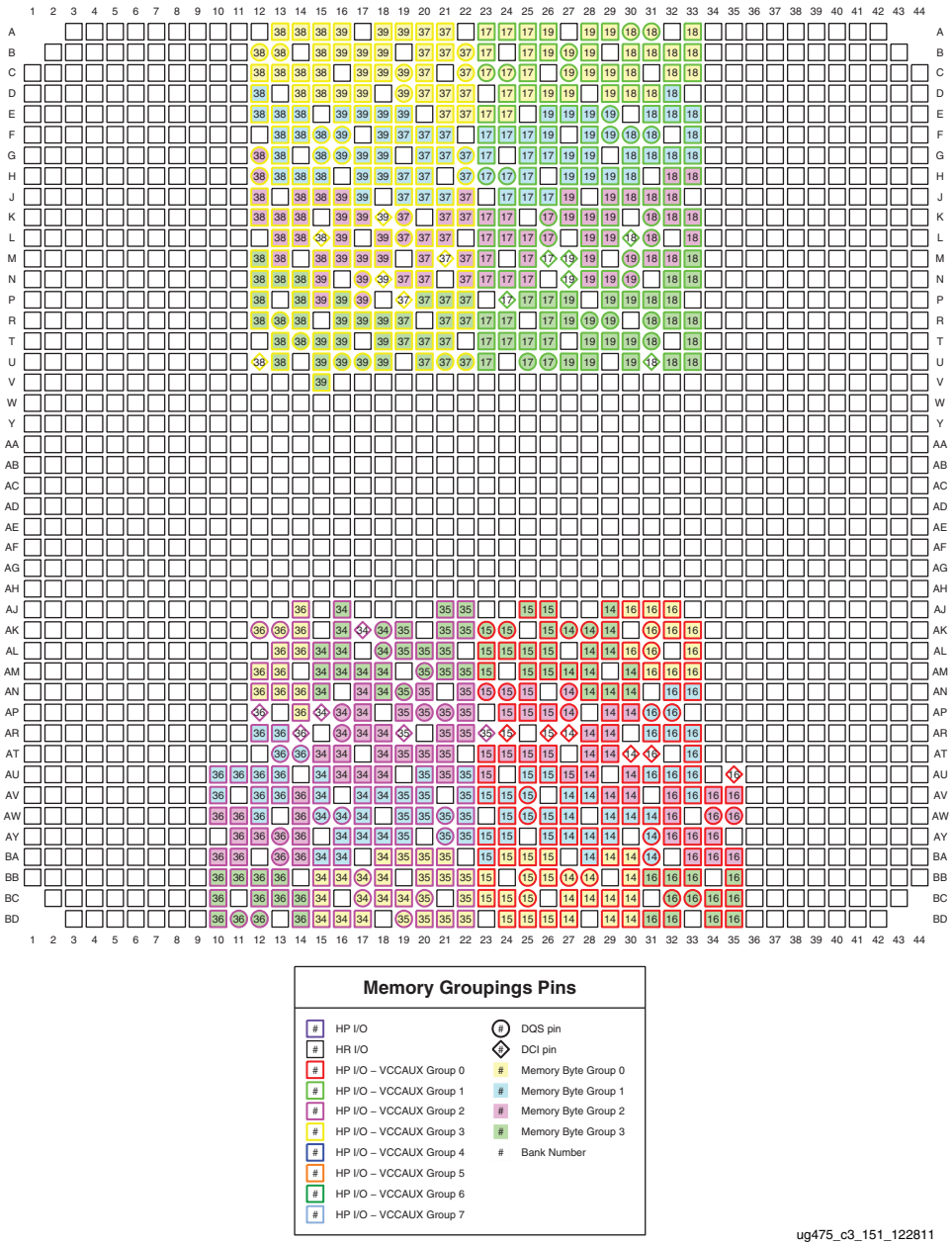


Figure 3-131: **FFG1927 Package—XC7VX550T and XC7VX690T Memory Groupings**

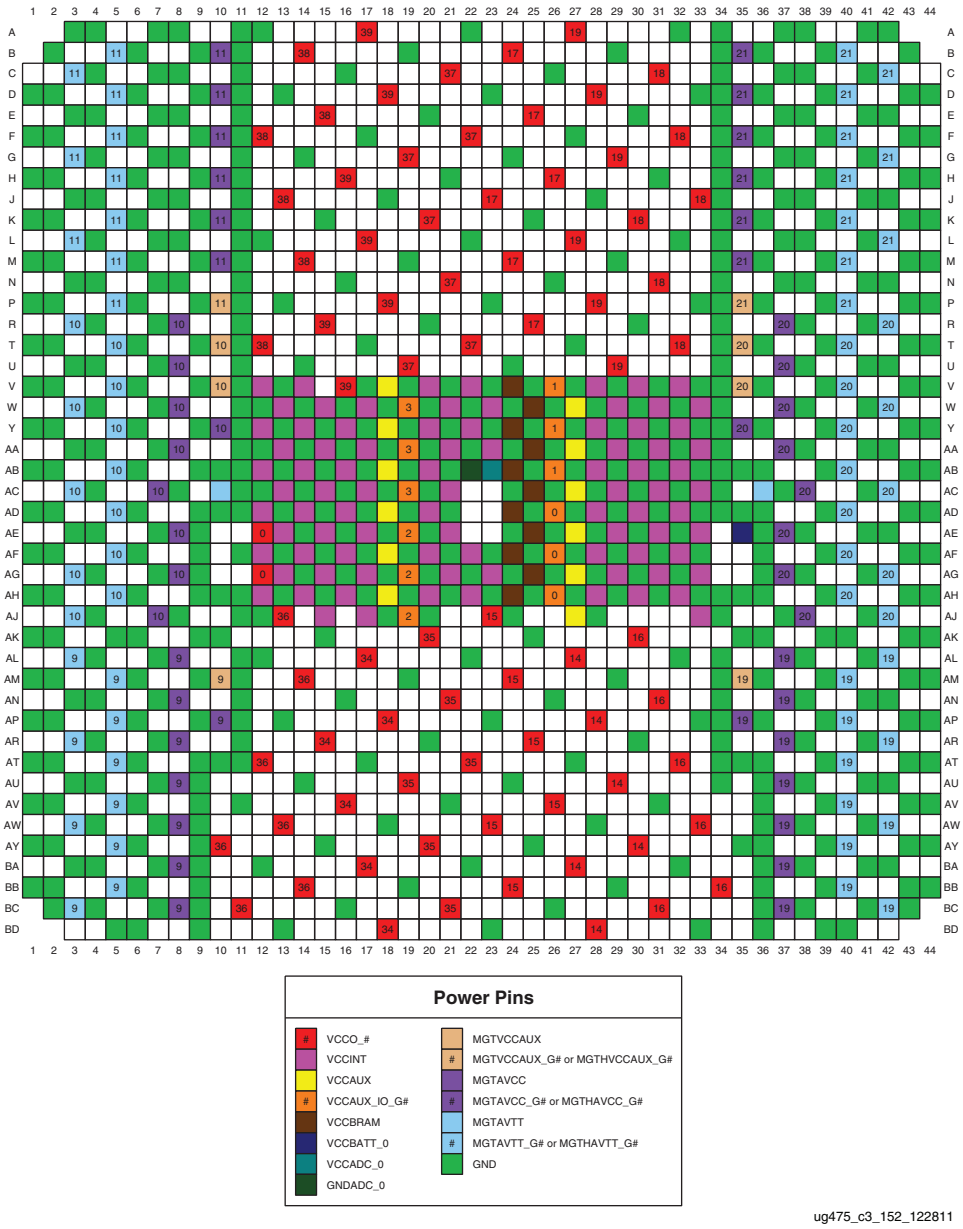


Figure 3-132: **FFG1927 Package—XC7VX550T and XC7VX690T Power and GND Placement**

FFG1930 Package—XC7VX690T

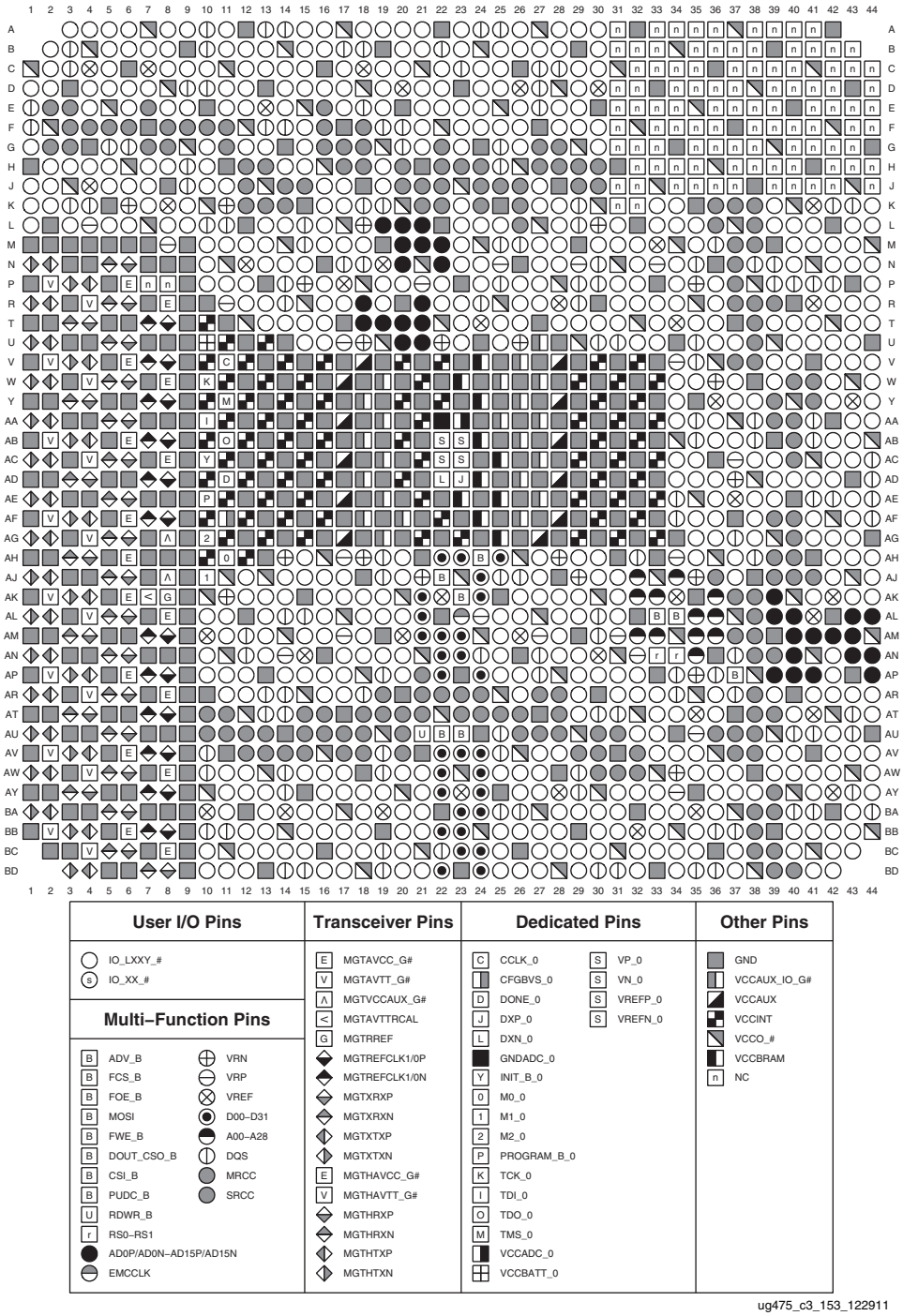


Figure 3-133: **FFG1930 Package—XC7VX690T Pinout Diagram**

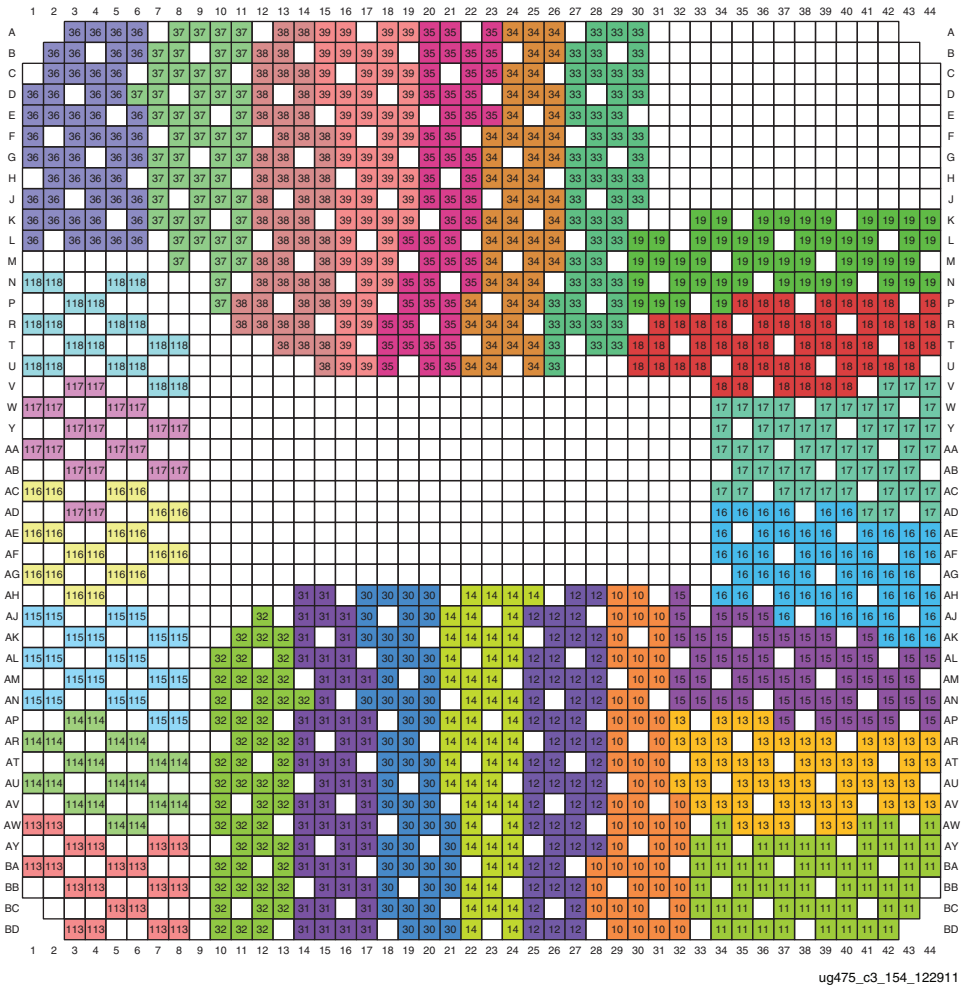


Figure 3-134: **FFG1930 Package—XC7VX690T I/O Banks**

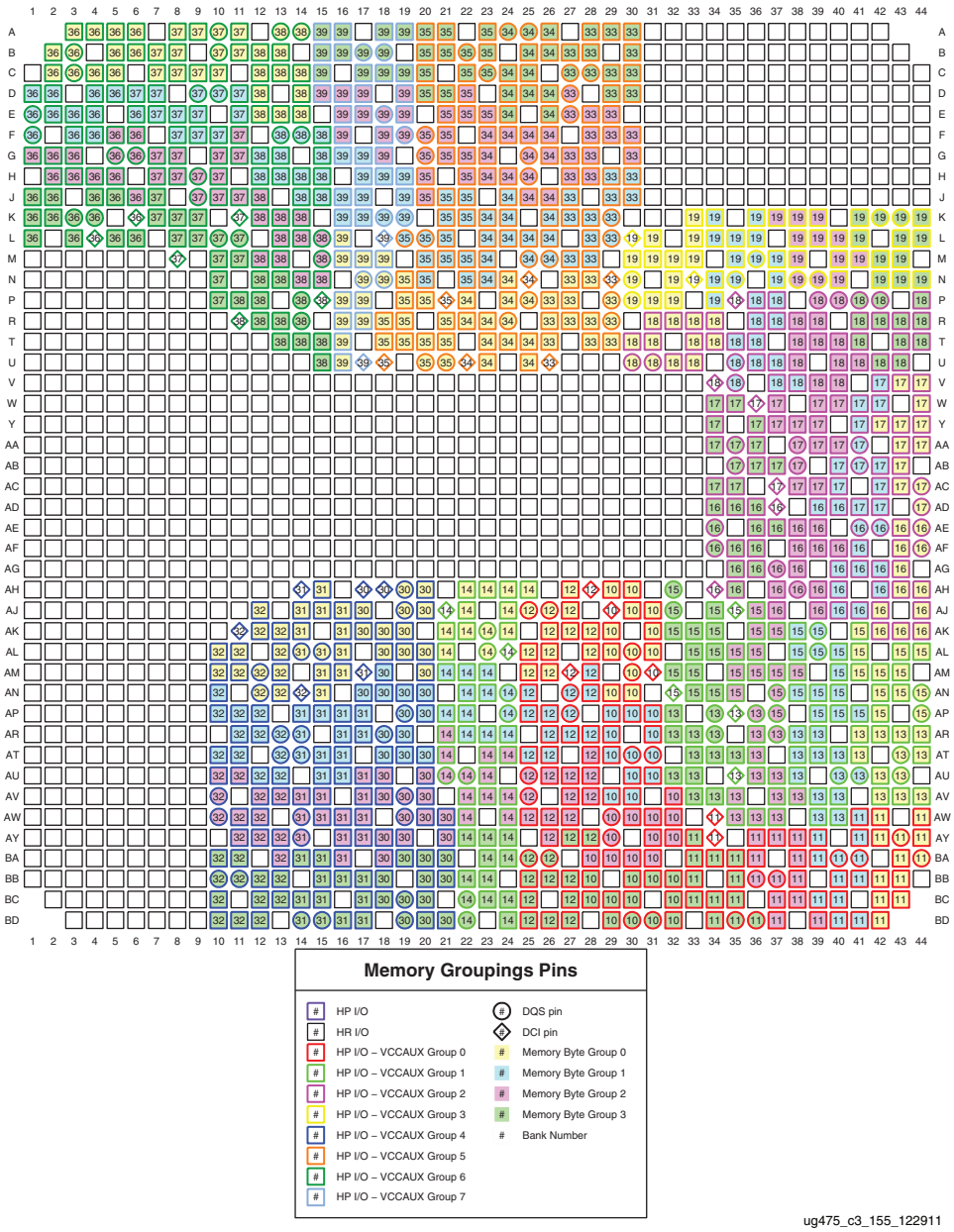


Figure 3-135: **FFG1930 Package—XC7VX690T Memory Groupings**

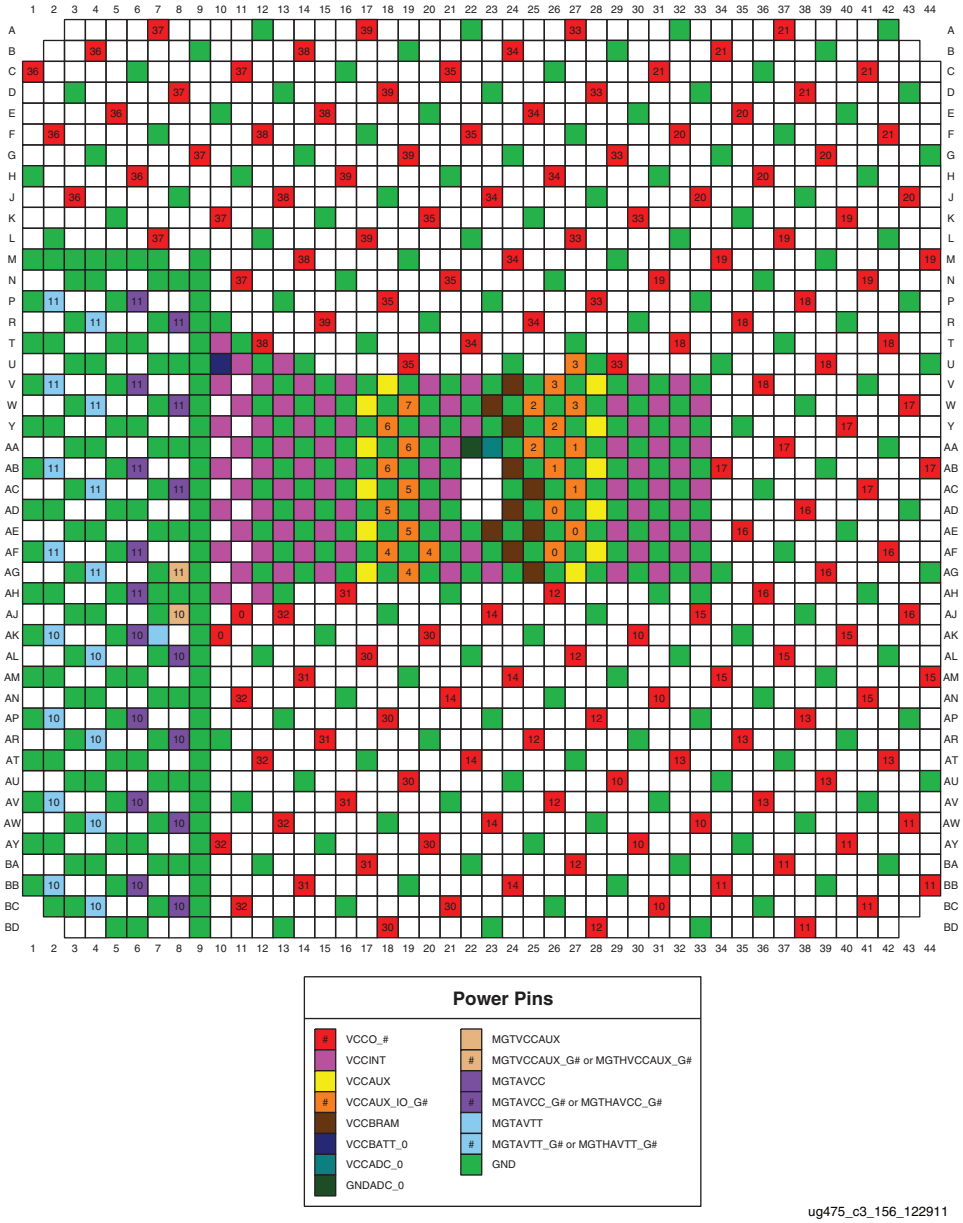


Figure 3-136: **FFG1930 Package—XC7VX690T Power and GND Placement**

FFG1928 Package—XC7VX980T

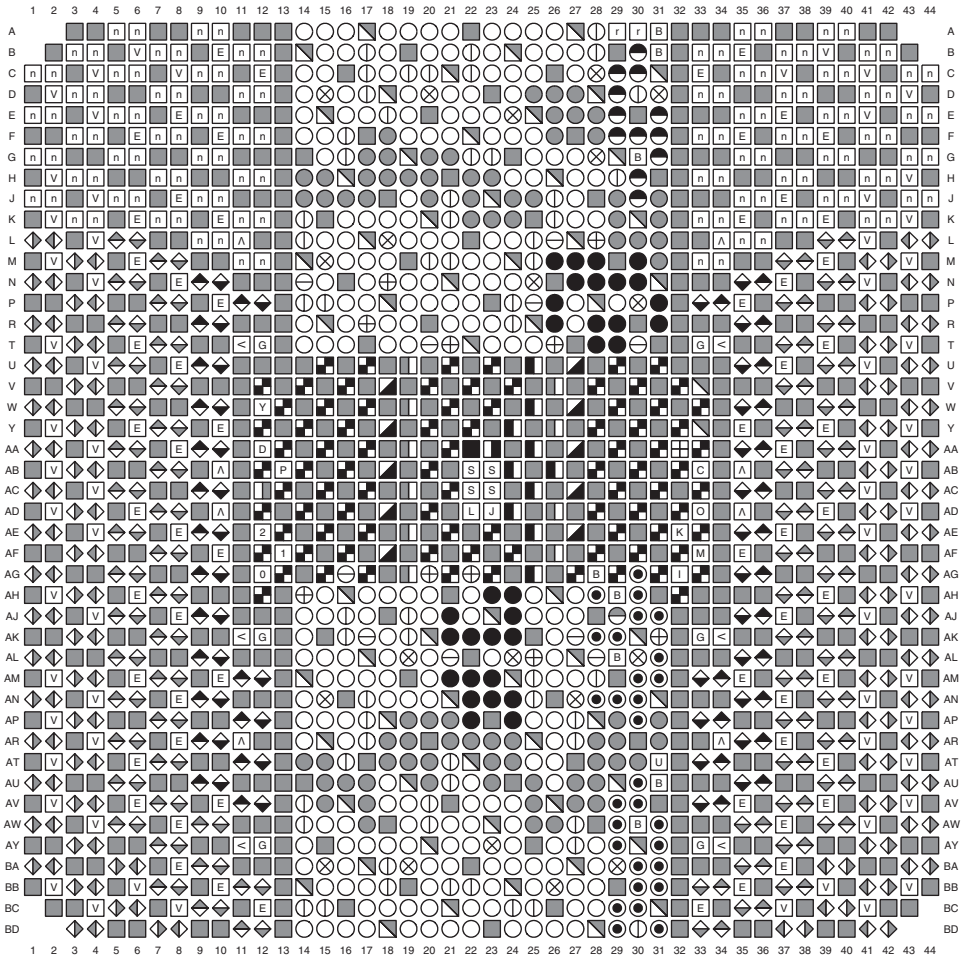


Figure 3-137: **FFG1928 Package—XC7VX980T Pinout Diagram**

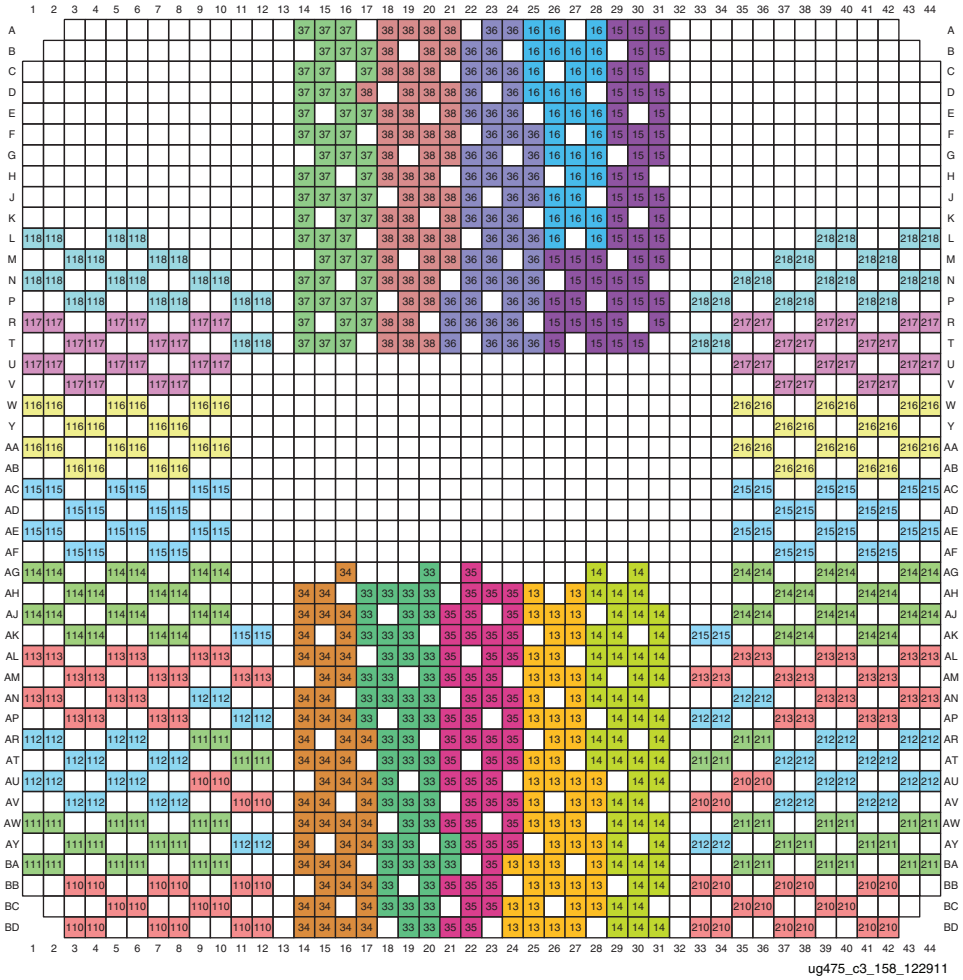


Figure 3-138: **FFG1928 Package—XC7VX980T I/O Banks**

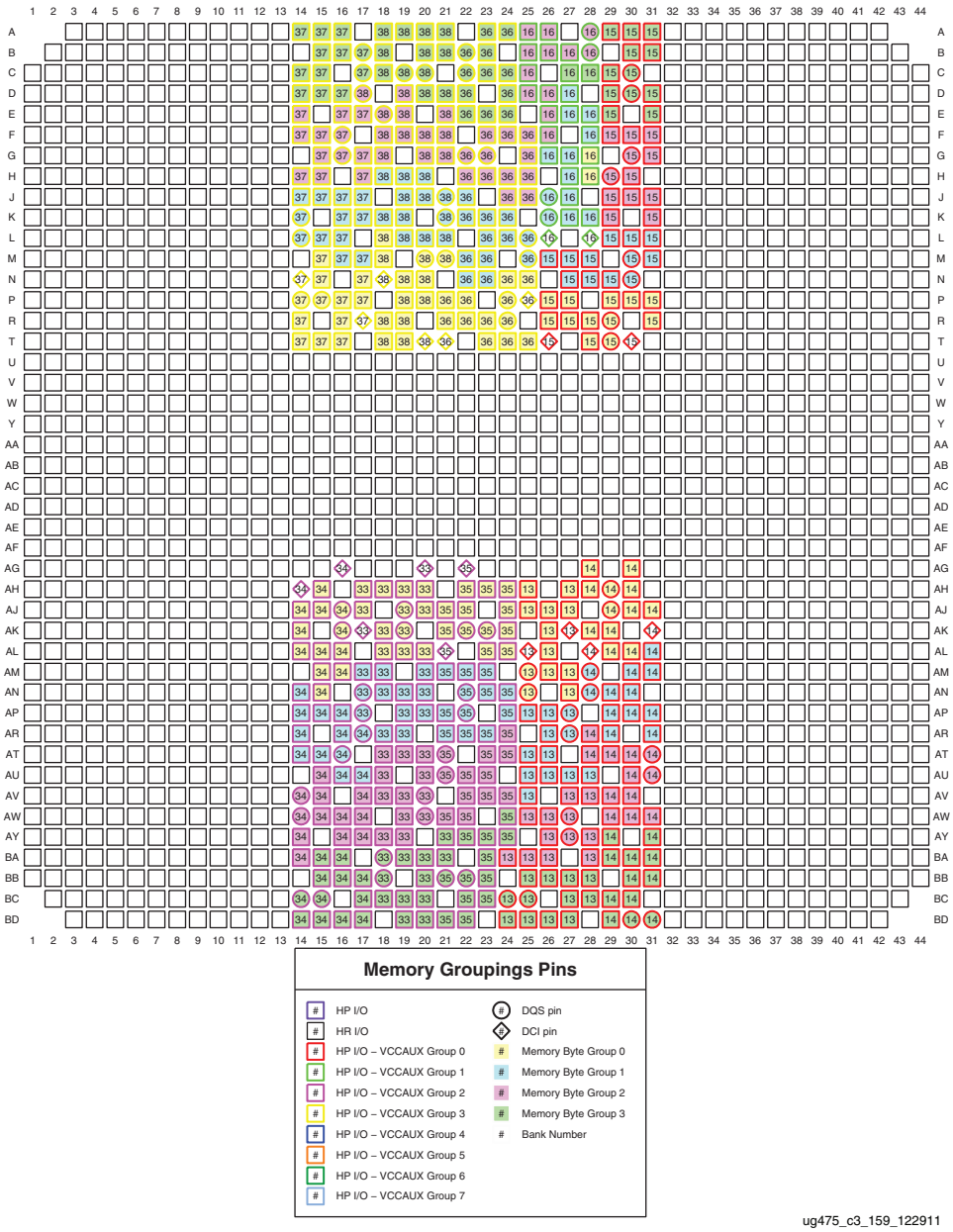


Figure 3-139: **FFG1928 Package—XC7VX980T Memory Groupings**

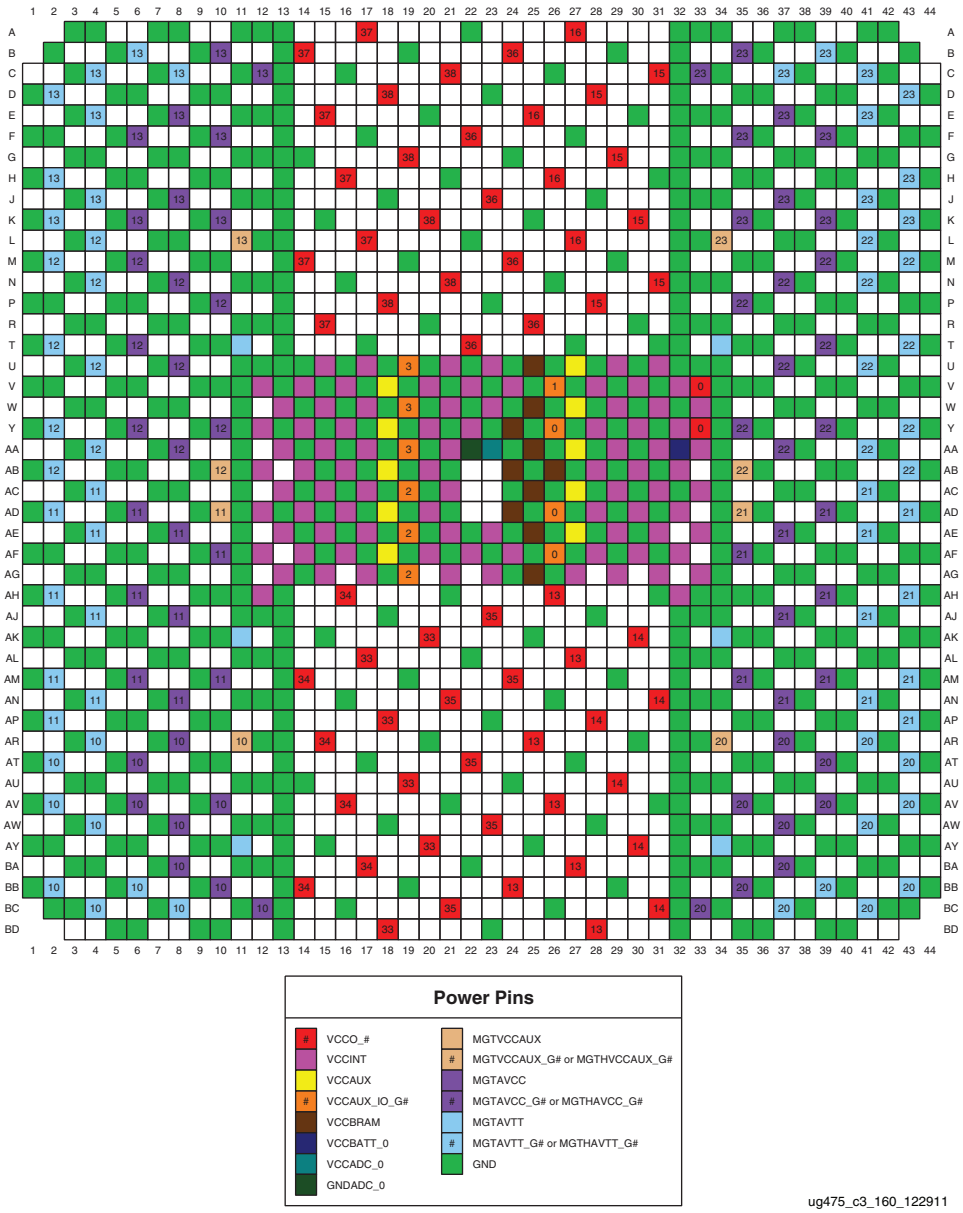


Figure 3-140: **FFG1928 Package—XC7VX980T Power and GND Placement**

FFG1930 Package—XC7VX980T

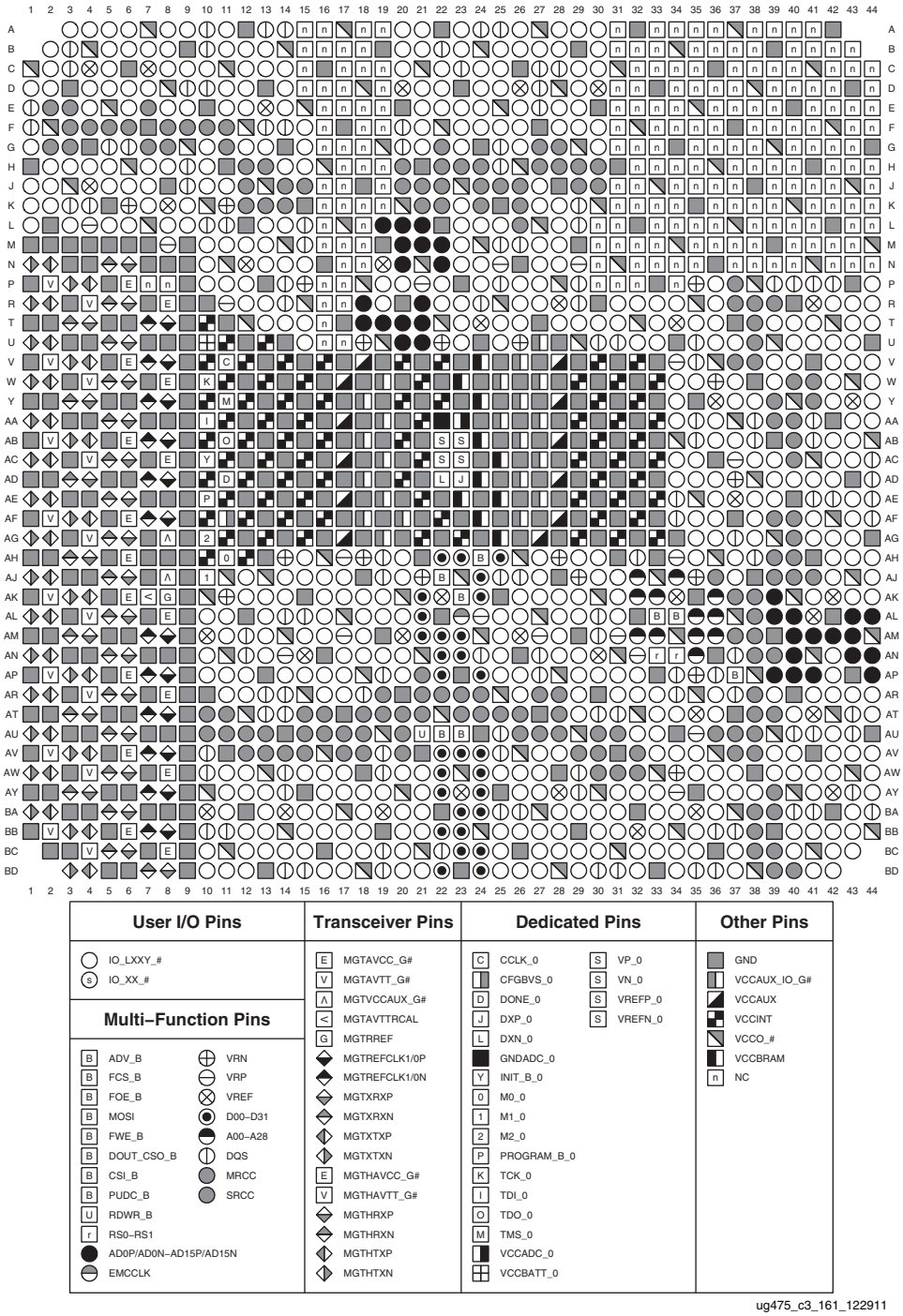


Figure 3-141: **FFG1930 Package—XC7VX980T Pinout Diagram**

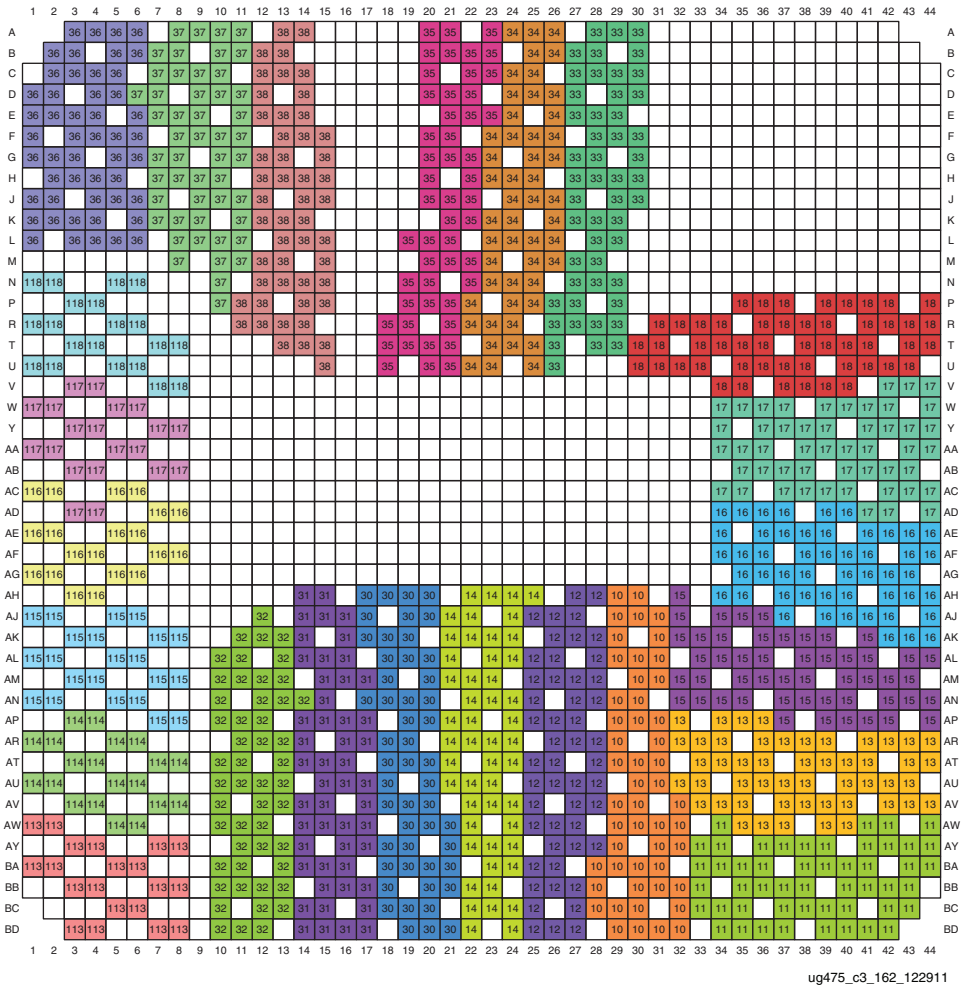


Figure 3-142: **FFG1930 Package—XC7VX980T I/O Banks**

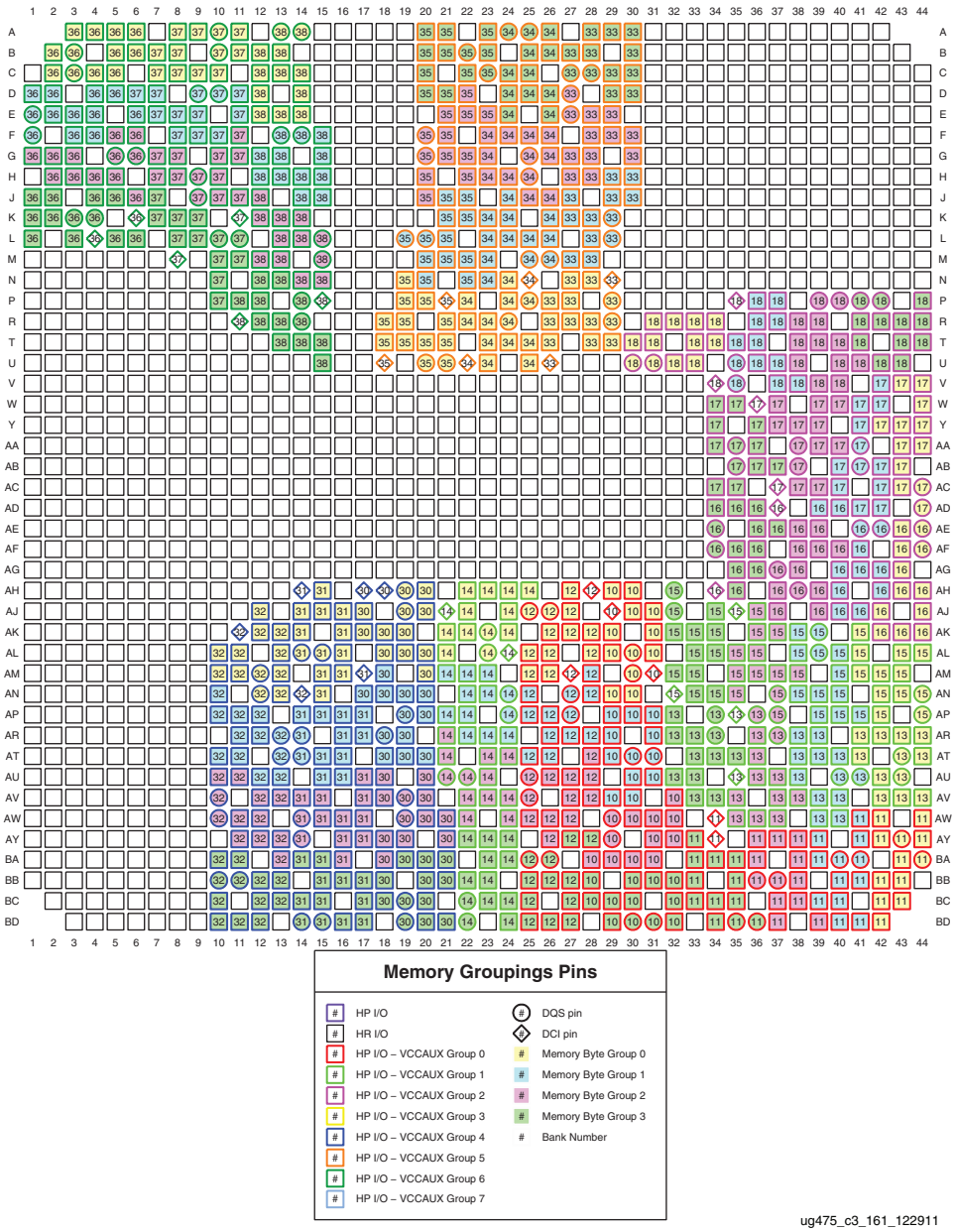


Figure 3-143: **FFG1930 Package—XC7VX980T Memory Groupings**

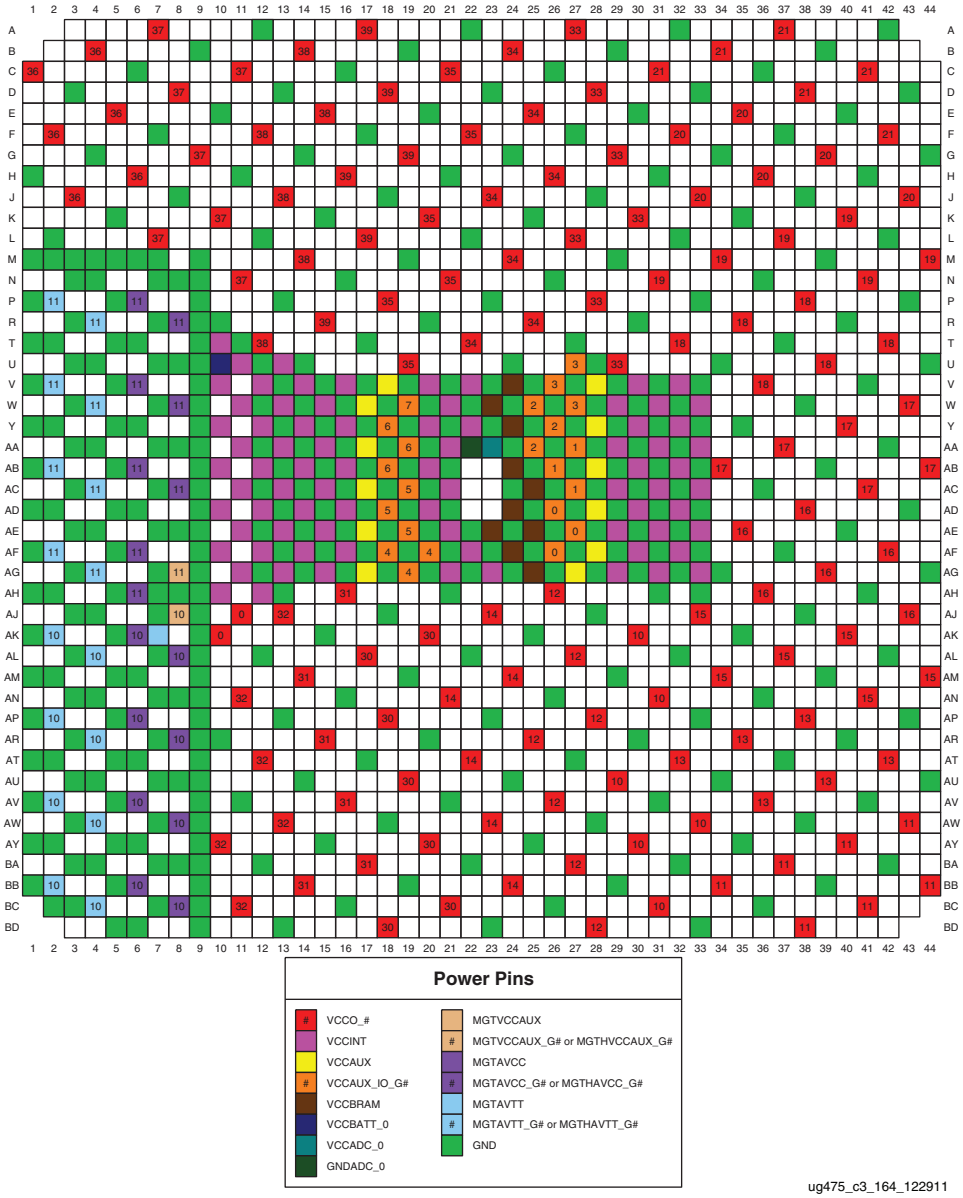
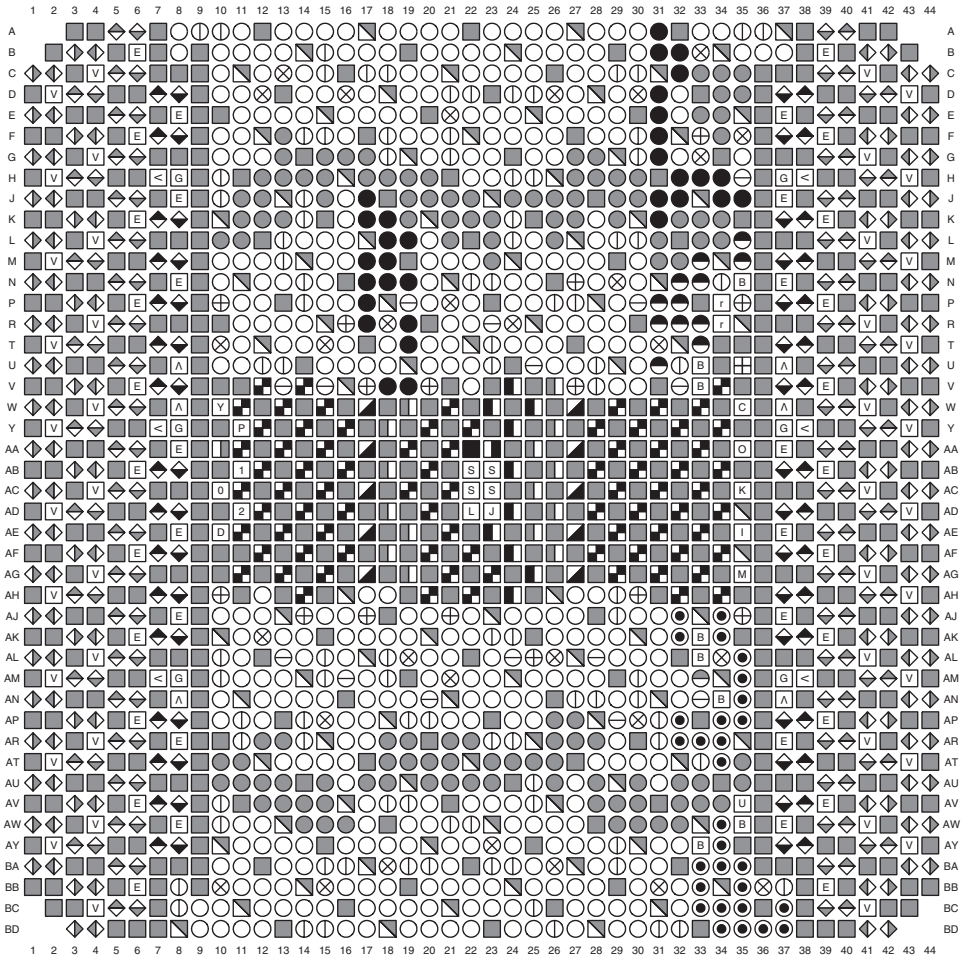


Figure 3-144: **FFG1930 Package—XC7VX980T Power and GND Placement**

FLG1926 Package—XC7VX1140T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	DONE_0	VCCAUX
ADV_B	MGTAVTTRCAL	DXP_0	VCCINT
FCS_B	MGTRREF	DXN_0	VCCO_#
FOE_B	MGTREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	MGTREFCLK1/0N	INIT_B_0	NC
FWE_B	MGTXRXP	M0_0	
DOUT_CSO_B	MGTXRXN	M1_0	
CSI_B	MGTXTXP	M2_0	
PUDC_B	MGTXTXN	PROGRAM_B_0	
RDWR_B	MGTHAVCC_G#	TCK_0	
RS0–RS1	MGTHAVTT_G#	TDI_0	
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0	
EMCCLK	MGTHRXN	TMS_0	
VRN	MGTHTXP	VCCADC_0	
VRP	MGTHTXN	VCCBATT_0	
VREF		VP_0	
D00–D31		VN_0	
A00–A28		VREFP_0	
DQS		VREFN_0	
MRCC			
SRCC			

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Figure 3-145: **FLG1926 Package—XC7VX1140T Pinout Diagram**

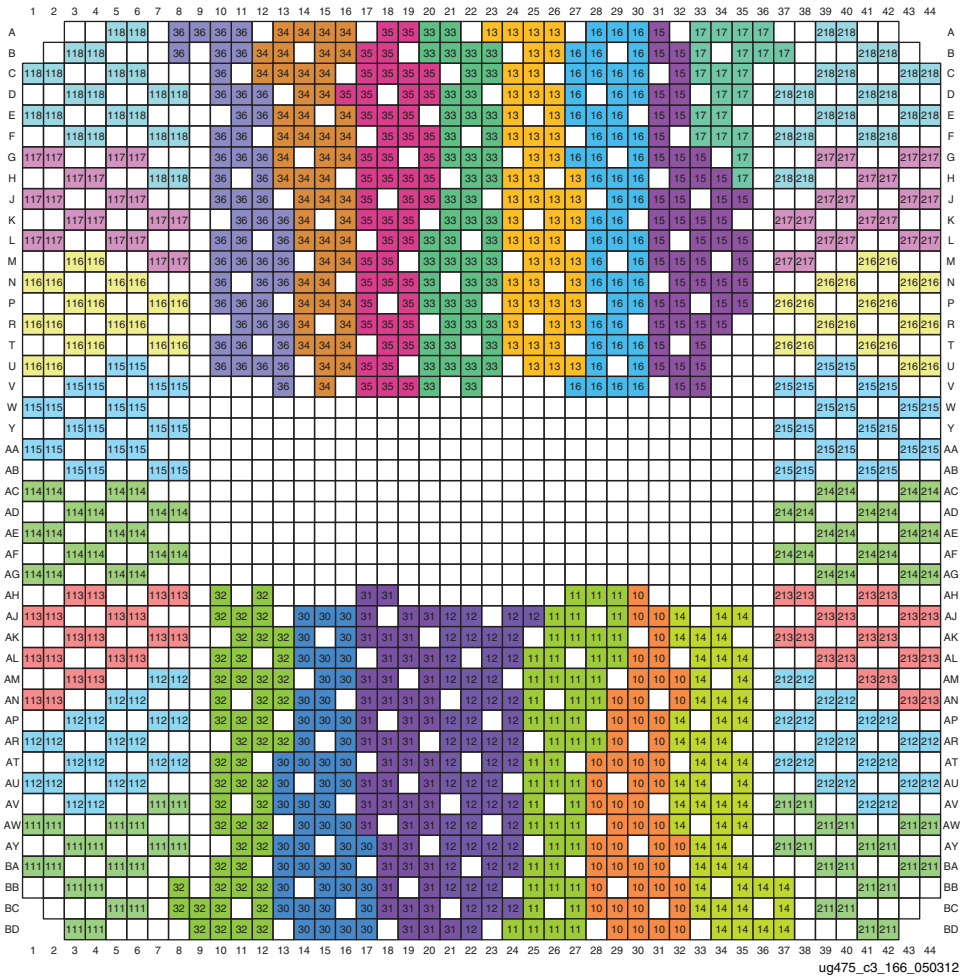

Figure 3-146: **FLG1926 Package—XC7VX1140T I/O Banks**

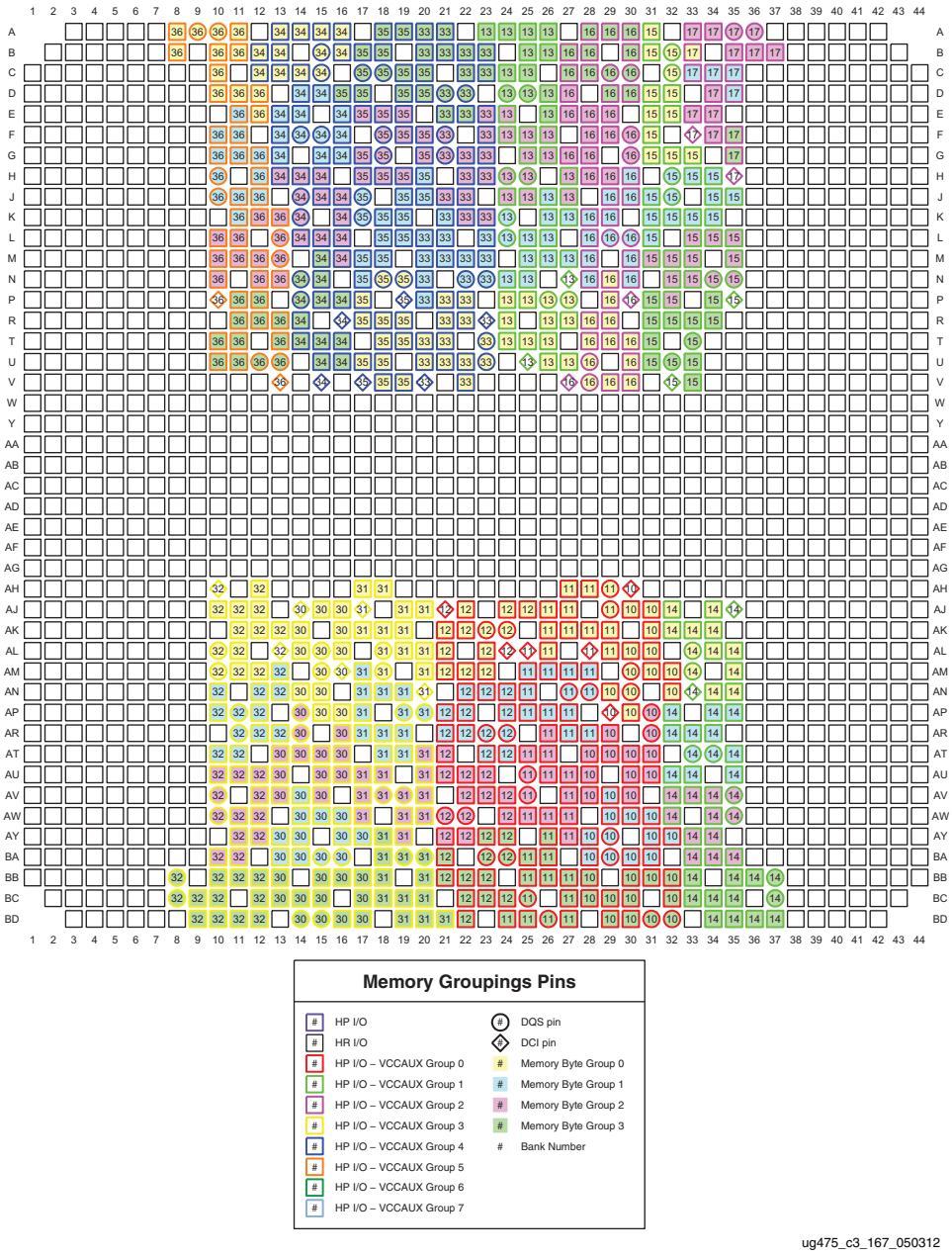

Figure 3-147: **FLG1926 Package—XC7VX1140T Memory Groupings**

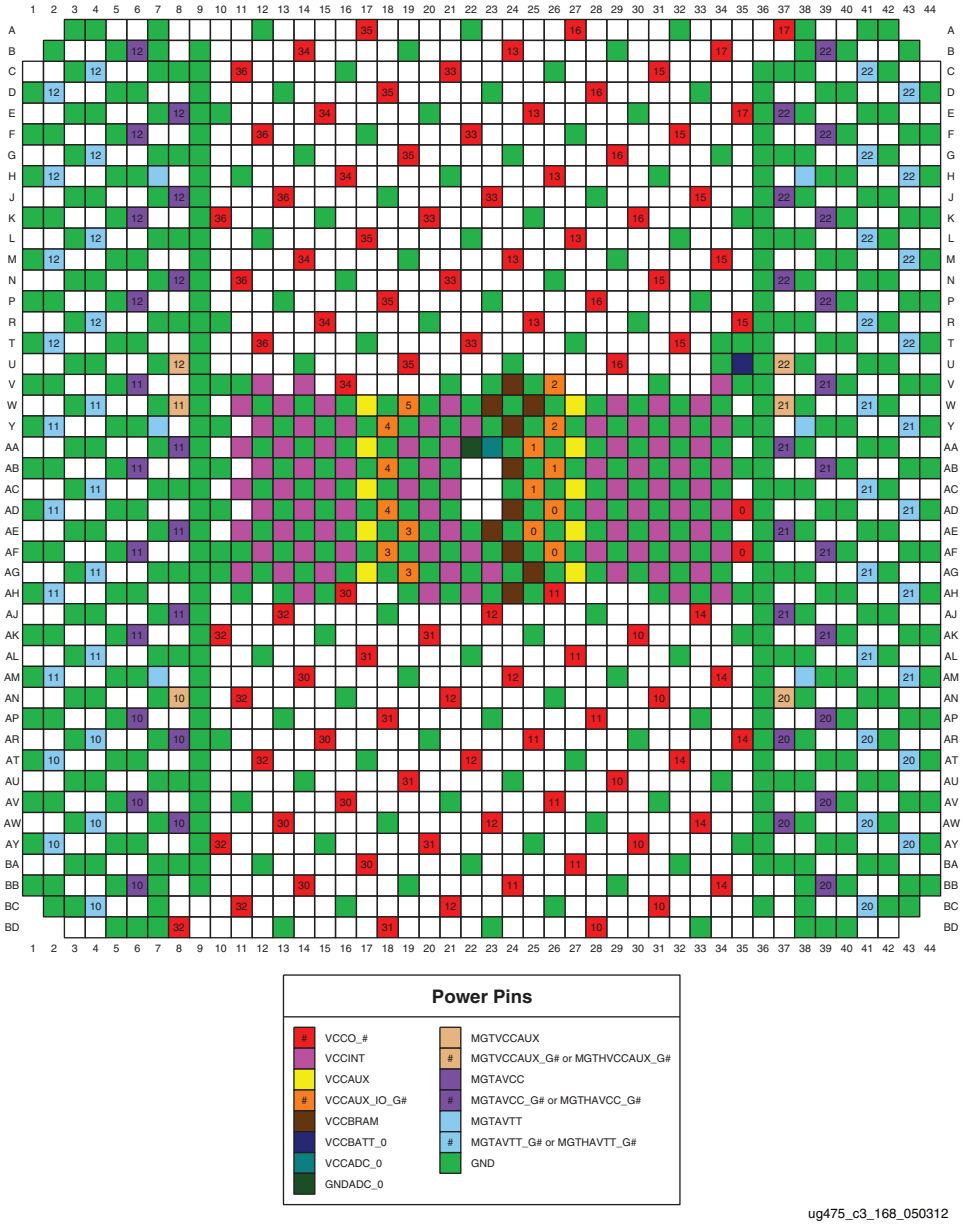

Figure 3-148: **FLG1926 Package—XC7VX1140T Power and GND Placement**

FLG1928 Package—XC7VX1140T

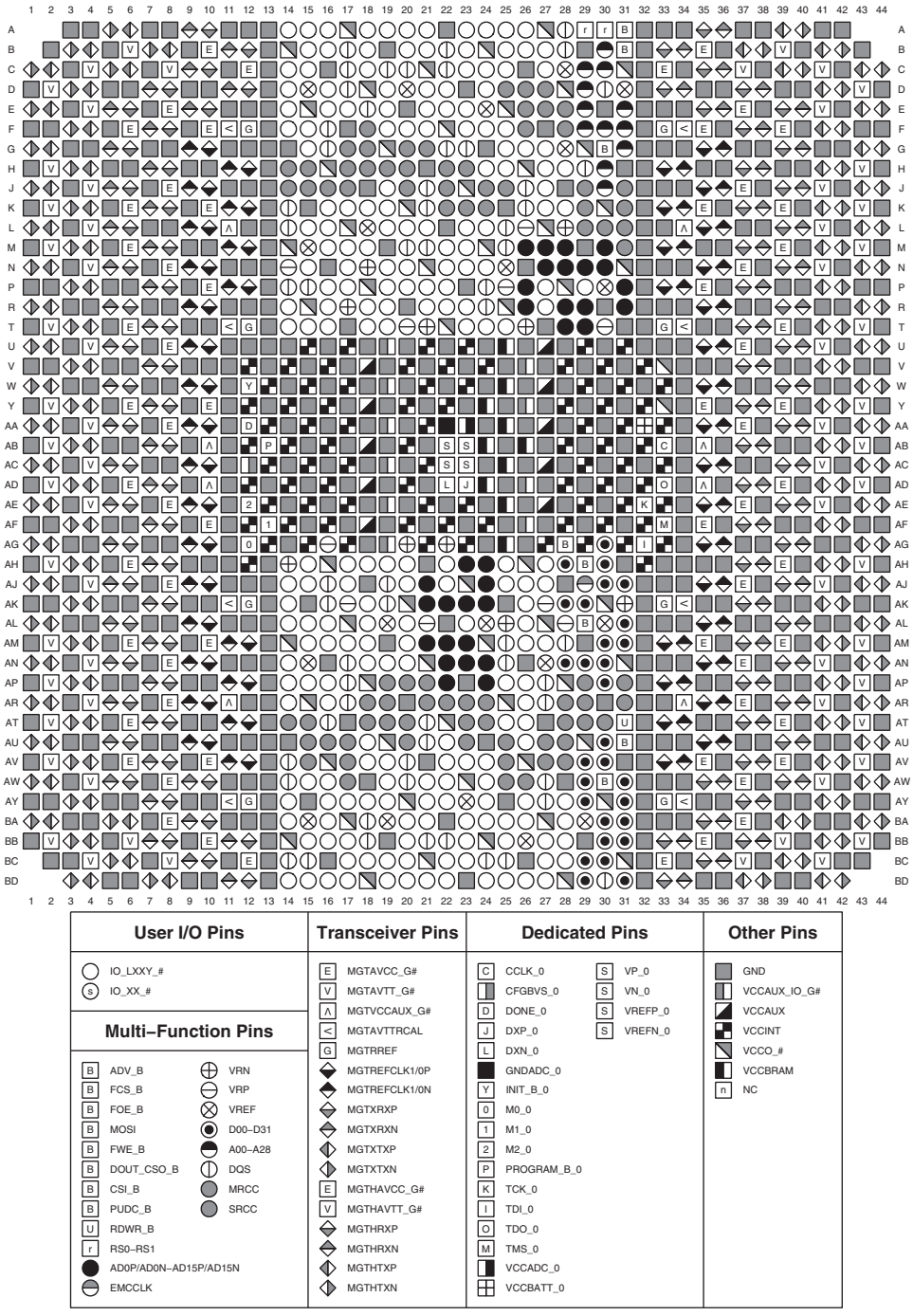

Figure 3-149: **FLG1928 Package—XC7VX1140T Pinout Diagram**

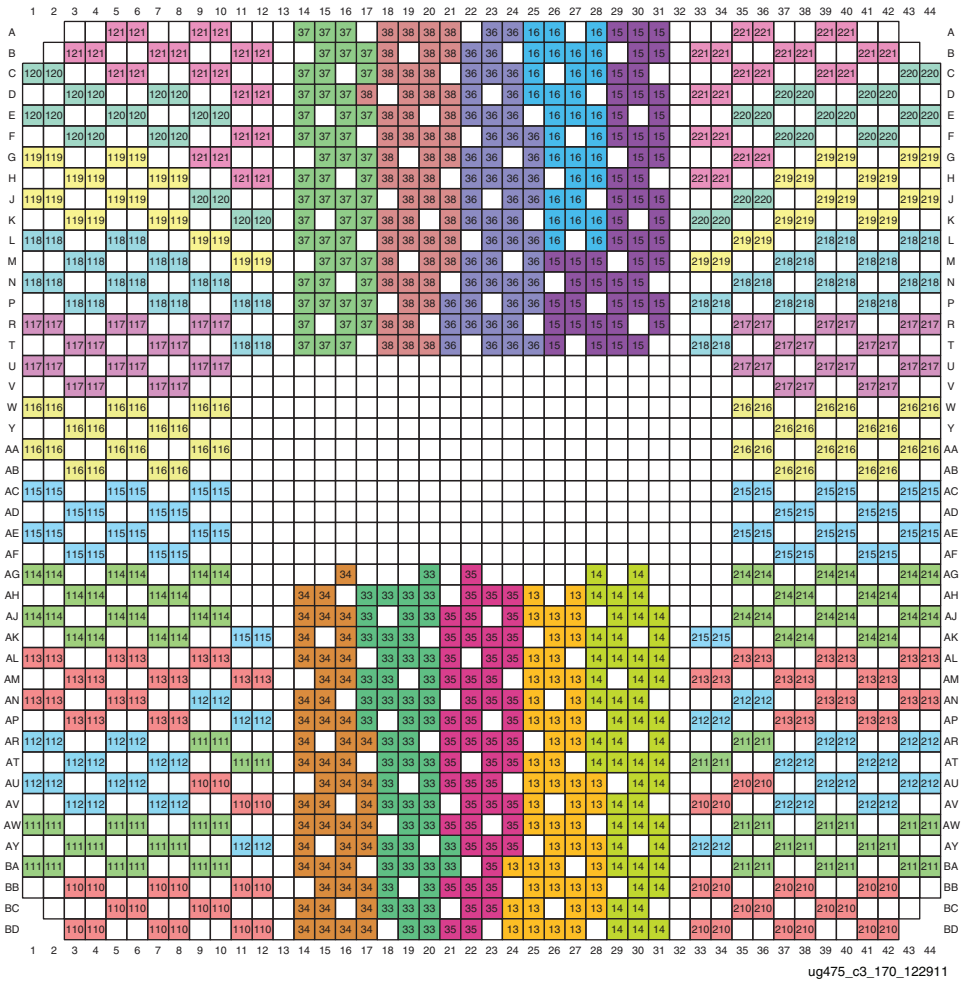

Figure 3-150: **FLG1928 Package—XC7VX1140T I/O Banks**

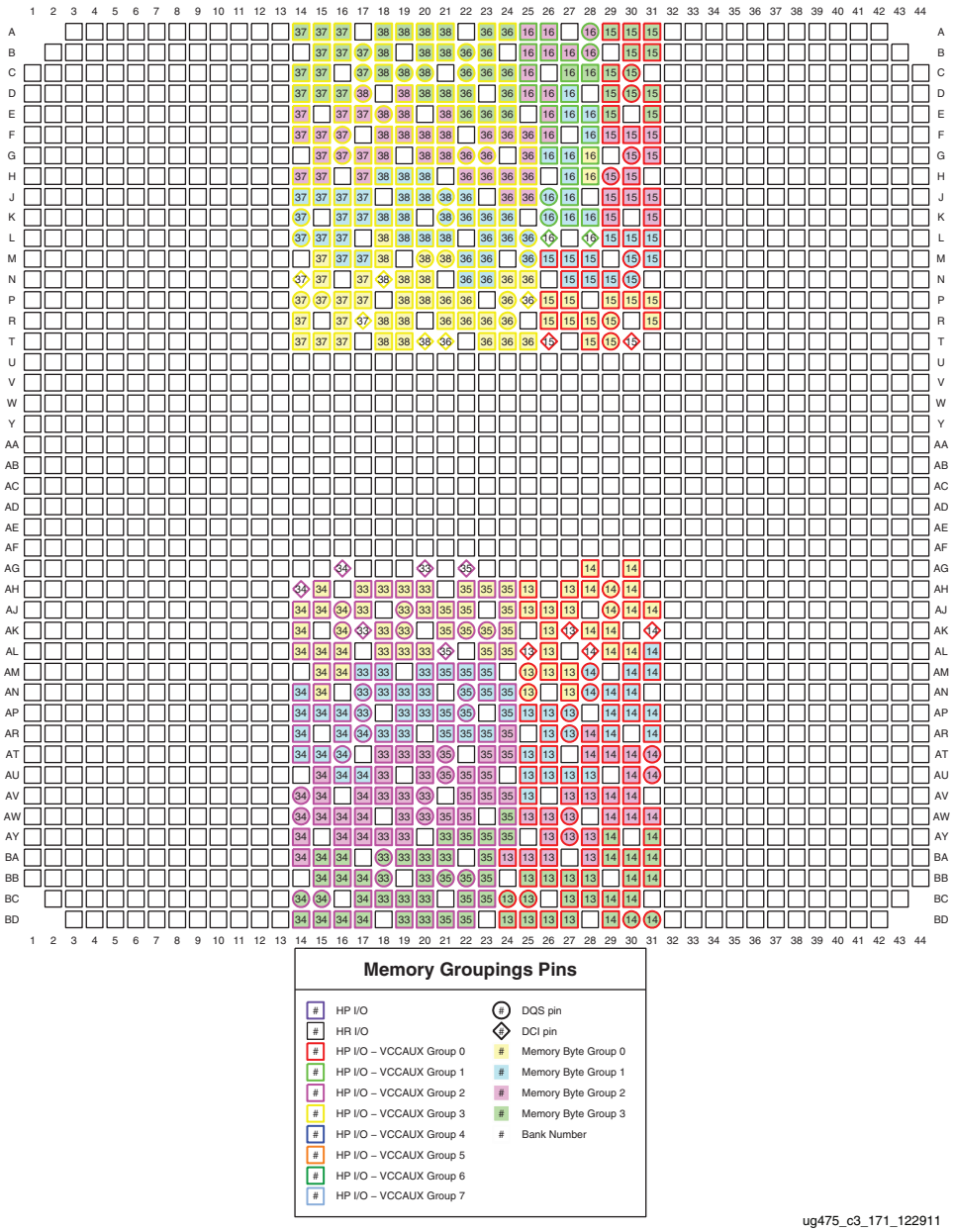

Figure 3-151: **FLG1928 Package—XC7VX1140T Memory Groupings**

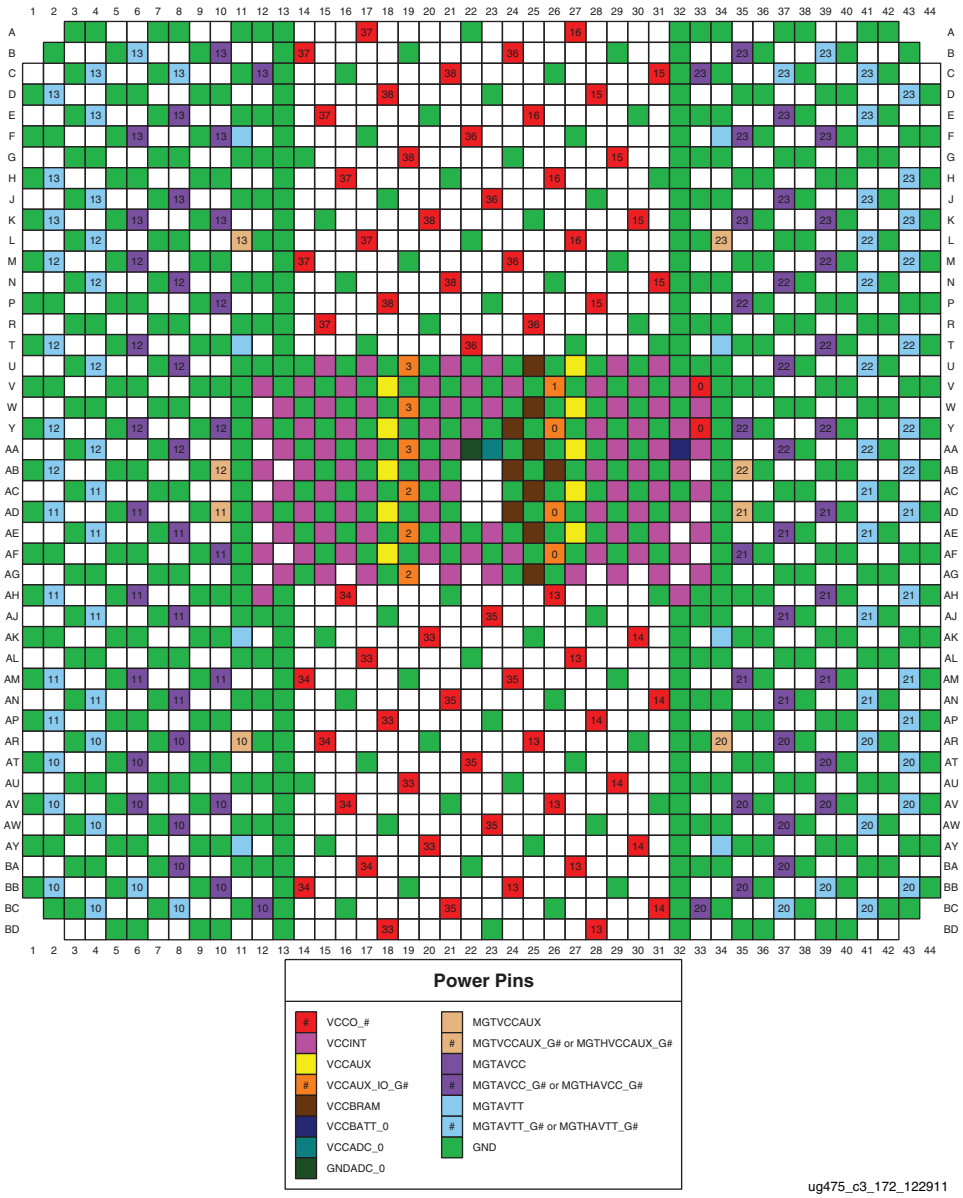

Figure 3-152: **FLG1928 Package—XC7VX1140T Power and GND Placement**

FLG1930 Package—XC7VX1140T

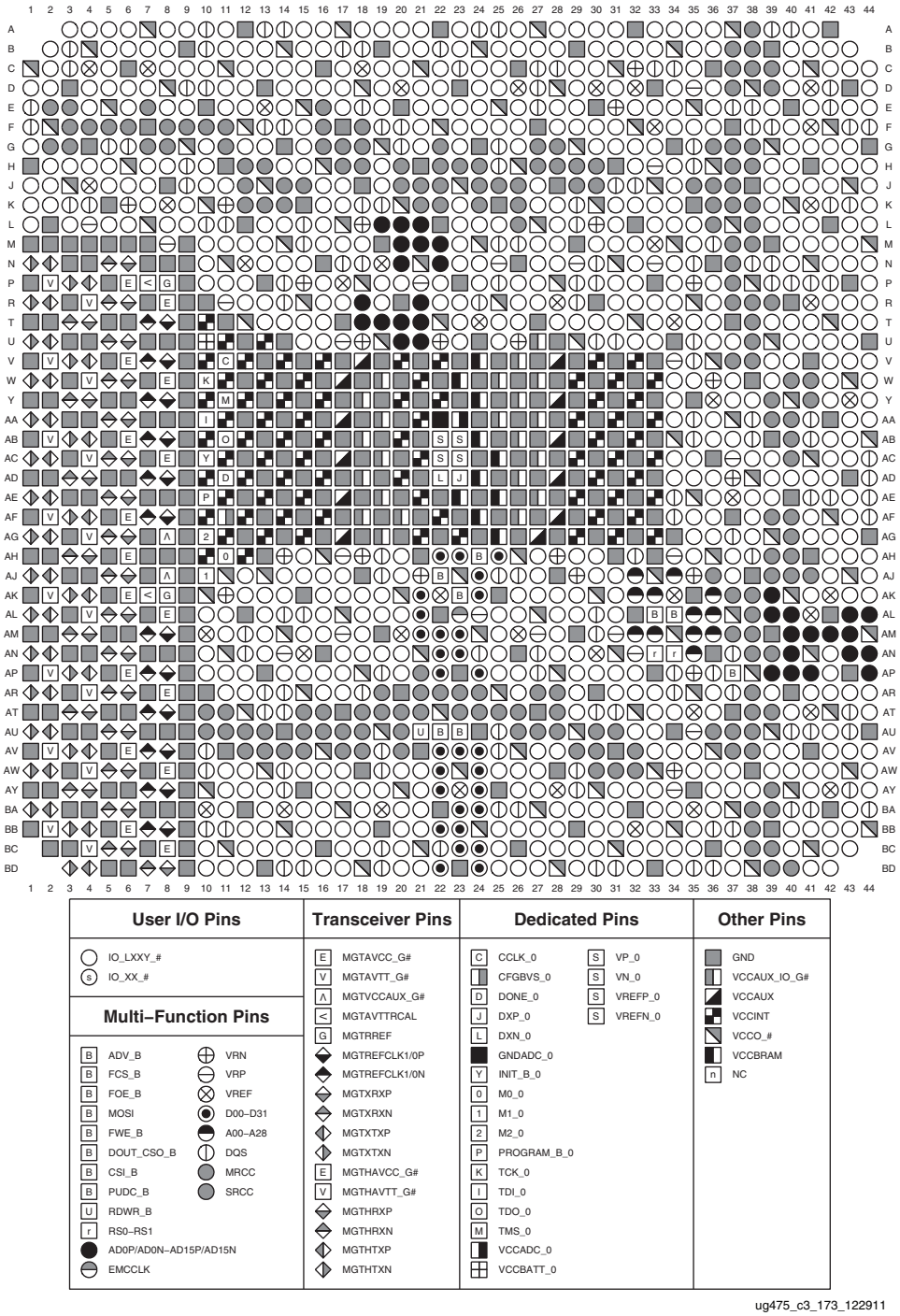

Figure 3-153: **FLG1930 Package—XC7VX1140T Pinout Diagram**

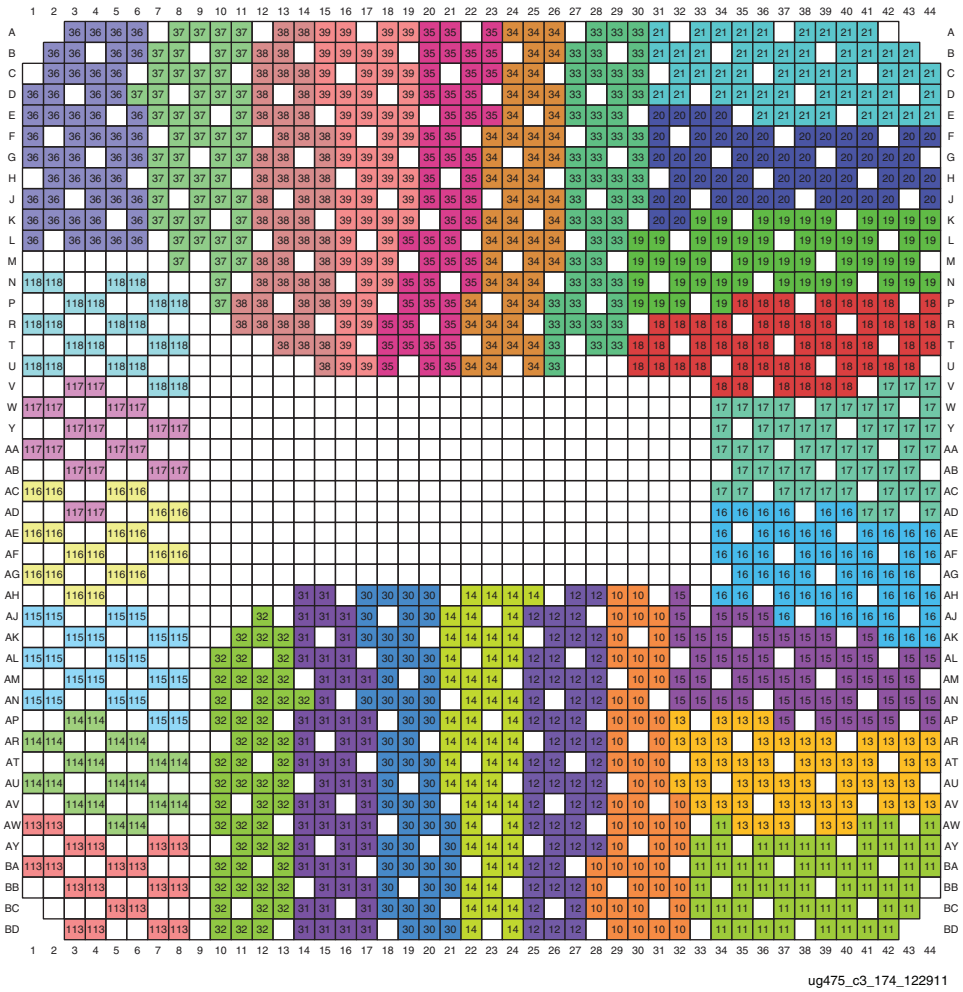

Figure 3-154: **FLG1930 Package—XC7VX1140T I/O Banks**

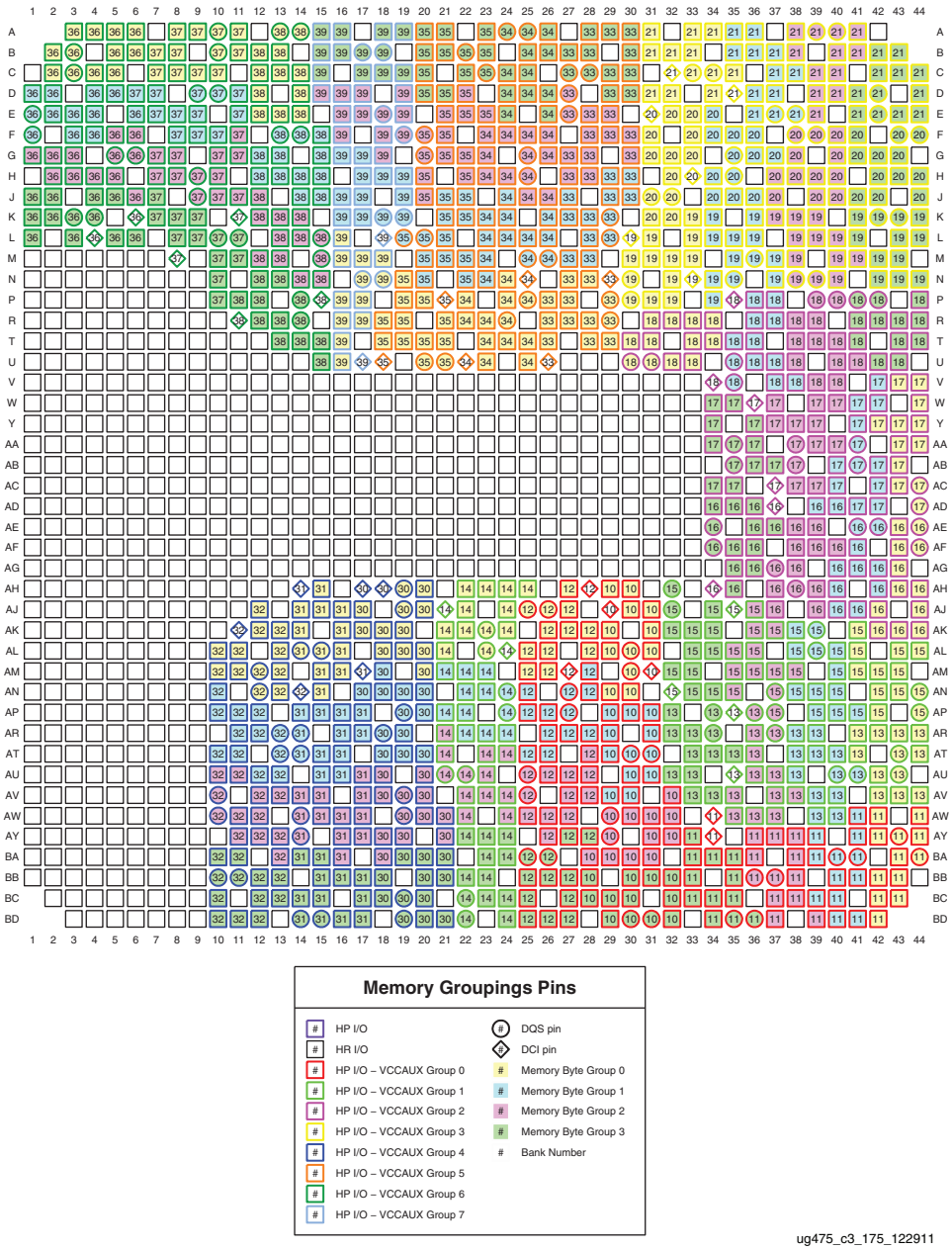

Figure 3-155: **FLG1930 Package—XC7VX1140T Memory Groupings**

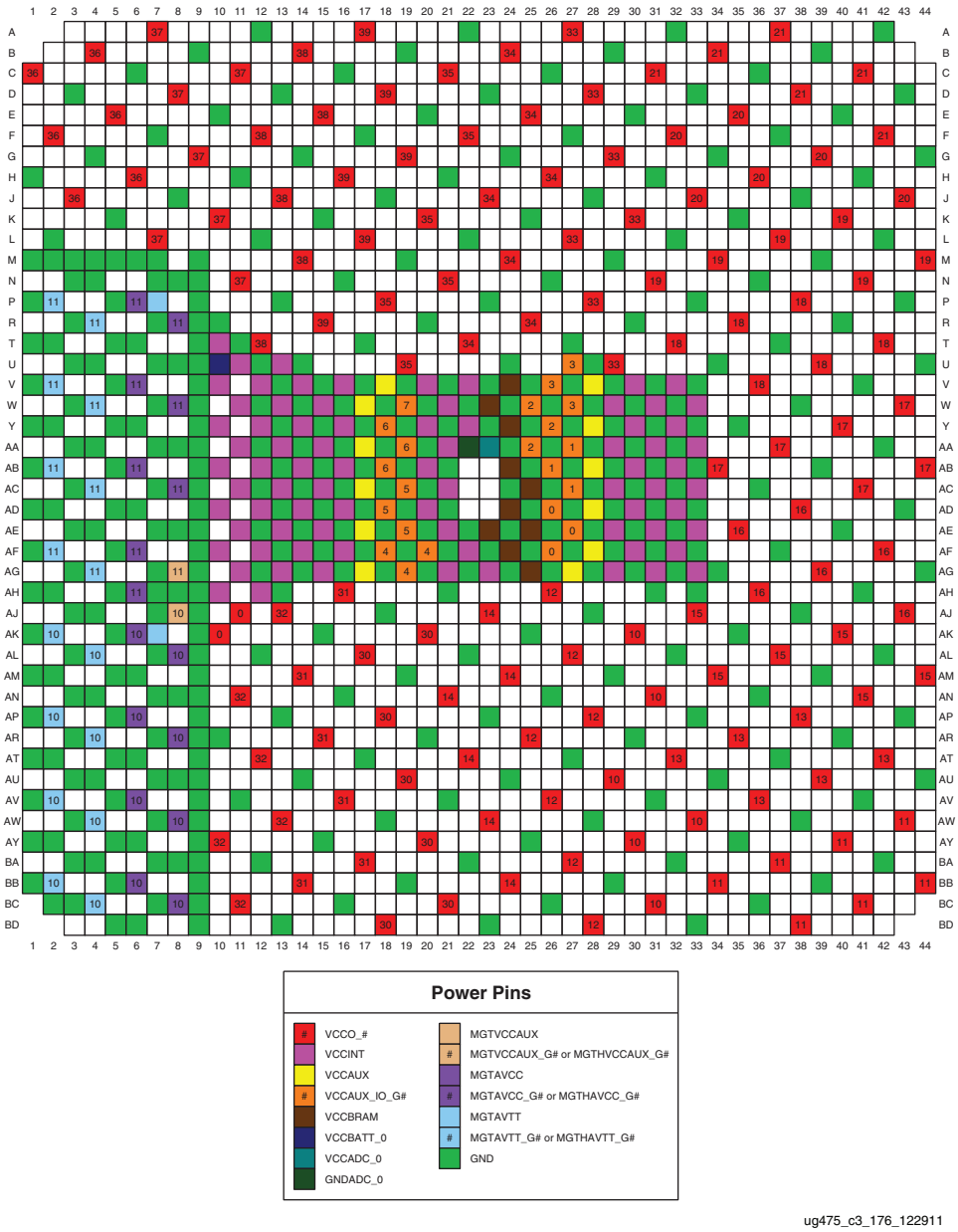

Figure 3-156: **FLG1930 Package—XC7VX1140T Power and GND Placement**

HCG1155 Package—XC7VH580T

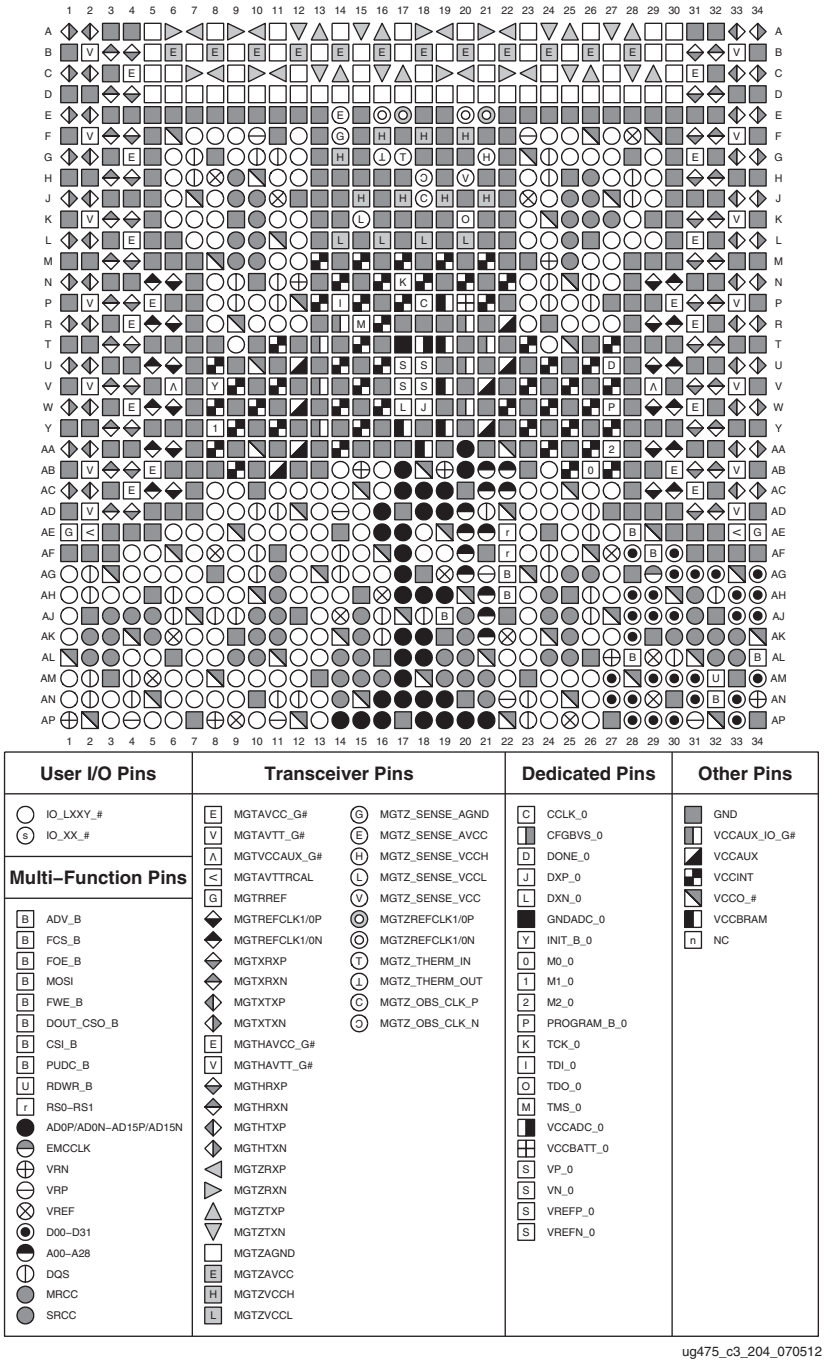

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Figure 3-157: **HCG1155 Package—XC7VH580T Pinout Diagram**

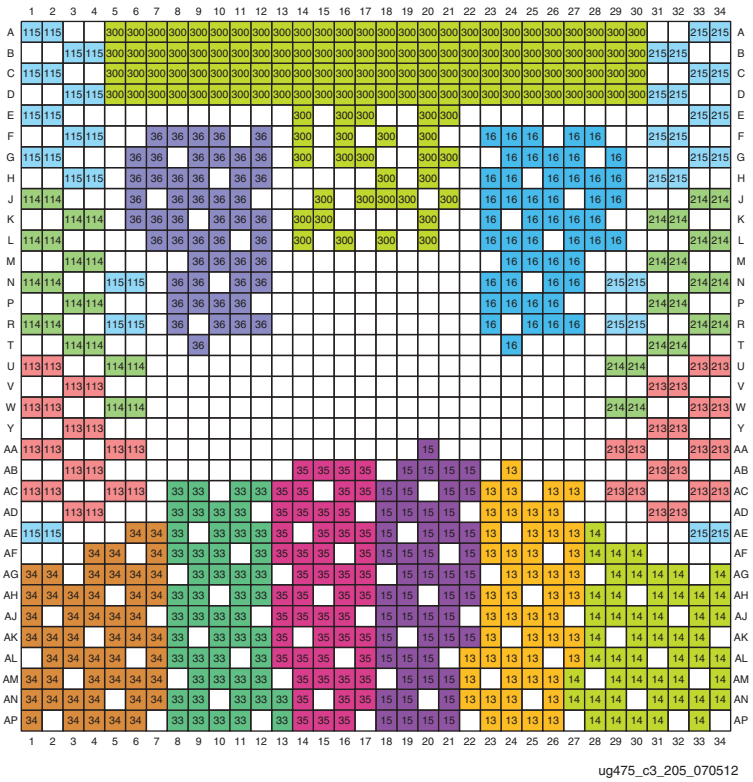


Figure 3-158: **HCG1155 Package—XC7VH580T I/O Banks**

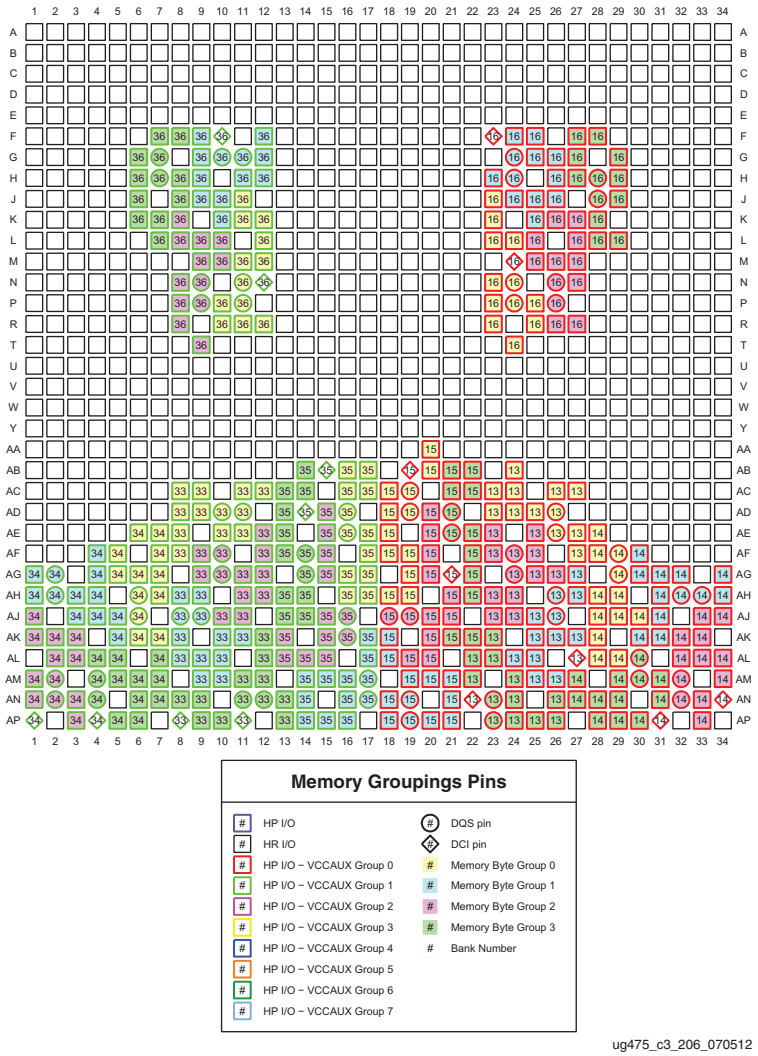


Figure 3-159: **HCG1155 Package—XC7VH580T Memory Groupings**

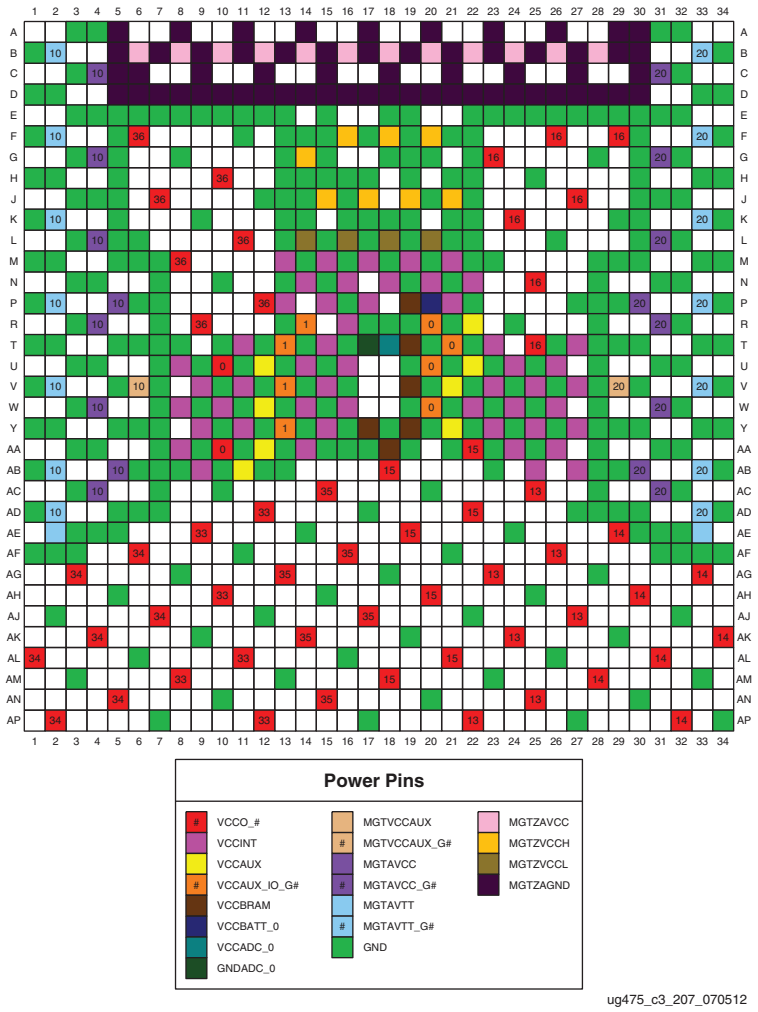
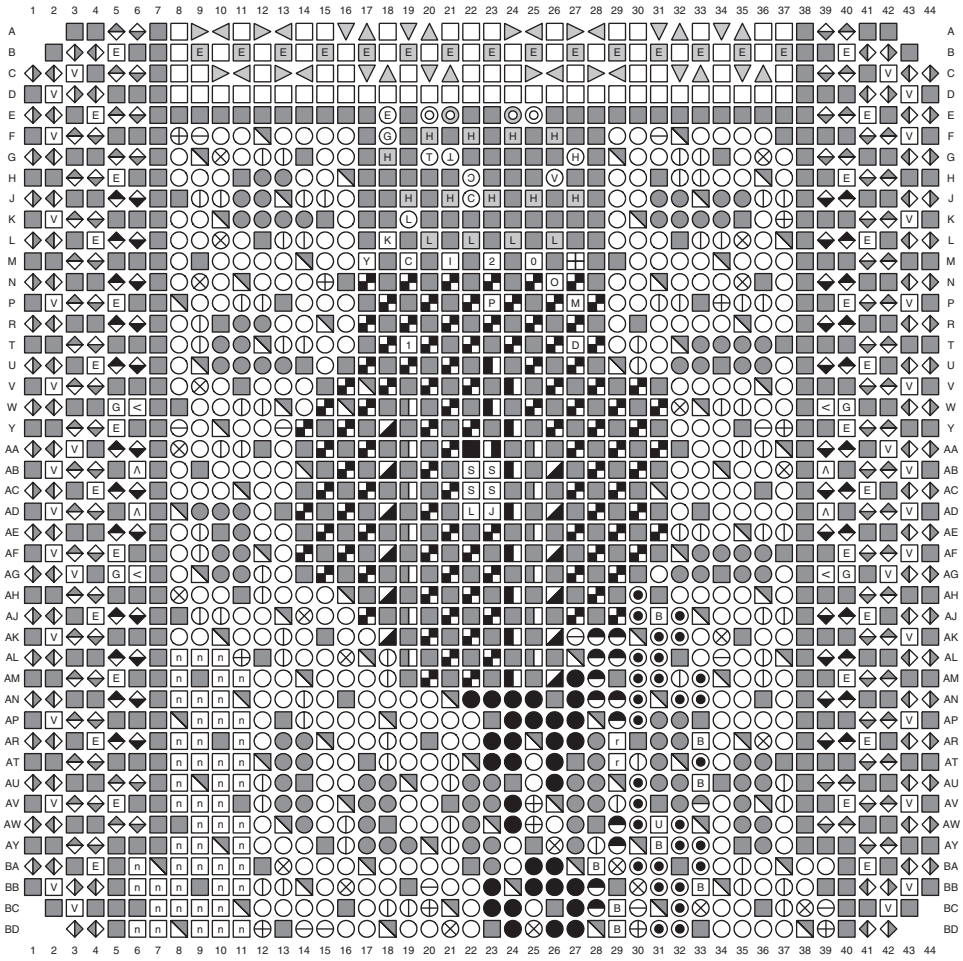


Figure 3-160: **HCG1155 Package—XC7VH580T Power and GND Placement**

HCG1931 Package—XC7VH580T



User I/O Pins	Transceiver Pins		Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	MGTZ_SENSE_AGND	CCLK_0	GND
IO_XX_#	MGTAVTT_G#	MGTZ_SENSE_AVCC	CFGBVS_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	MGTZ_SENSE_VCCH	DONE_0	VCCAUX
ADV_B	MGTAVTTRCAL	MGTZ_SENSE_VCCL	DXP_0	VCCINT
FCS_B	MGTRREF	MGTZ_SENSE_VCC	DXN_0	VCCO_#
FOE_B	MGTREFCLK1/0P	MGTZREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	MGTREFCLK1/0N	MGTZREFCLK1/0N	INIT_B_0	NC
FWE_B	MGTXRXP	MGTZ_THERM_IN	M0_0	
DOUT_CSO_B	MGTXRXN	MGTZ_THERM_OUT	M1_0	
CSI_B	MGTXTXP	MGTZ_OBS_CLK_P	M2_0	
PUDC_B	MGTXTXN	MGTZ_OBS_CLK_N	PROGRAM_B_0	
RDWR_B	MGTHAVCC_G#		TCK_0	
RS0–RS1	MGTHAVTT_G#		TDI_0	
AD0P/AD0N–AD15P/AD15N	MGTHRXP		TDO_0	
EMCCLK	MGTHRXN		TMS_0	
VRN	MGTHTXP		VCCADC_0	
VRP	MGTHTXN		VCCBATT_0	
VREF	MGTZRXP		VP_0	
D00–D31	MGTZRXN		VN_0	
A00–A28	MGTZTXP		VREFP_0	
DQS	MGTZTXN		VREFN_0	
MRCC	MGTZAGND			
SRCC	MGTZAVCC			
	MGTZVCCH			
	MGTZVCCL			

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Figure 3-161: **HCG1931 Package—XC7VH580T Pinout Diagram**

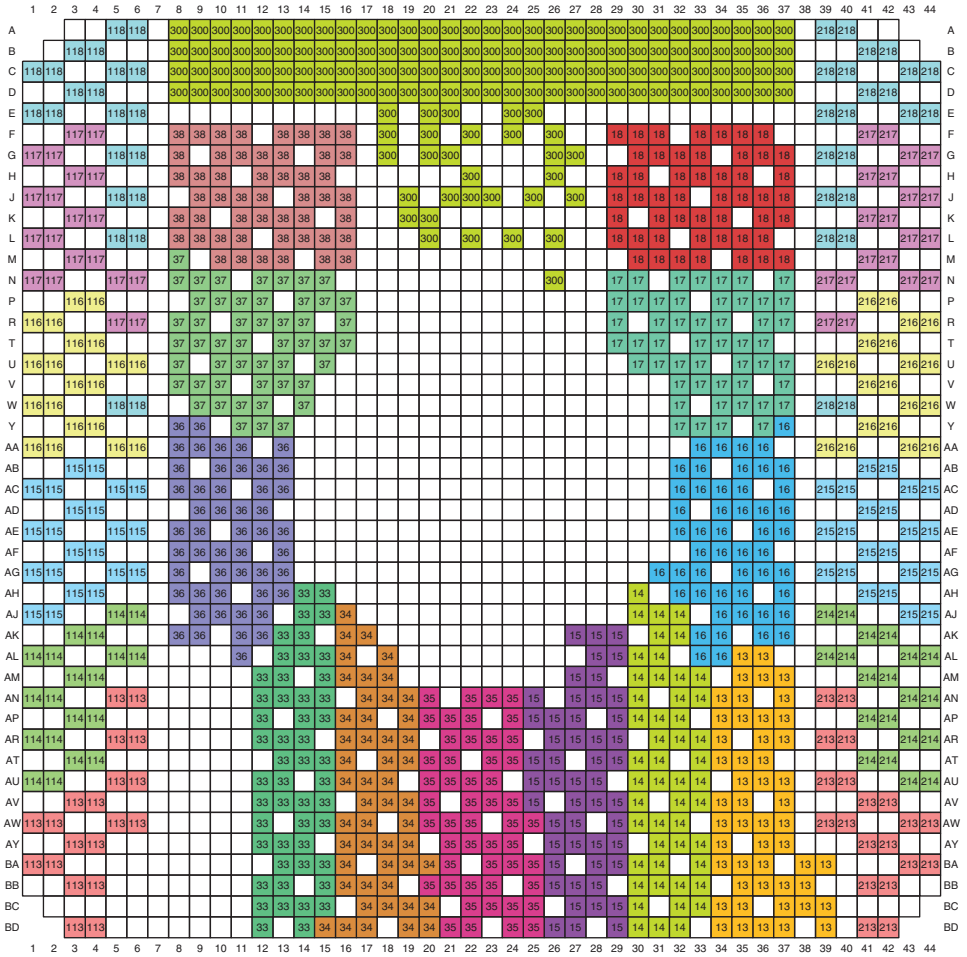


Figure 3-162: **HCG1931 Package—XC7VH580T I/O Banks**

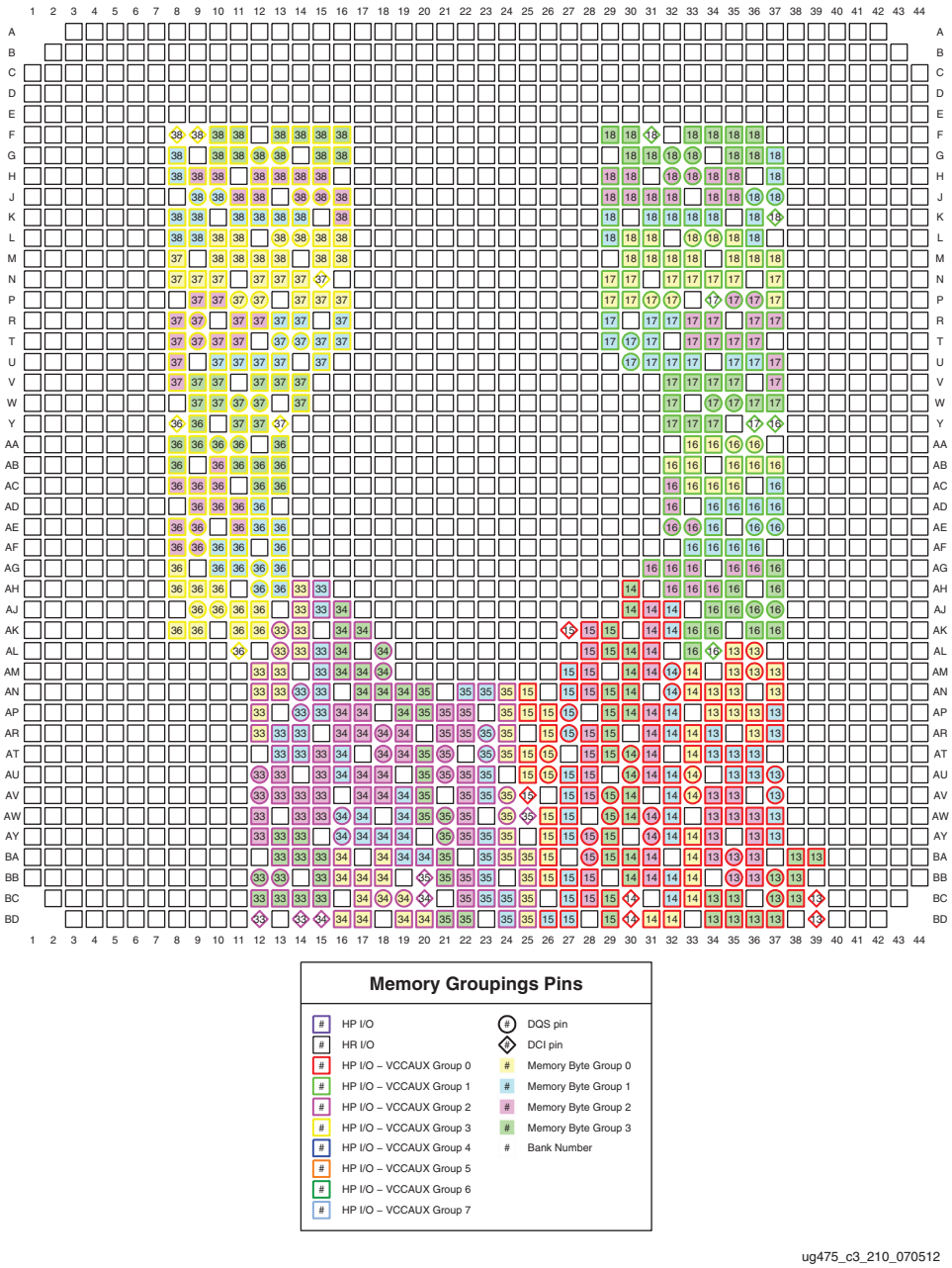


Figure 3-163: **HCG1931 Package—XC7VH580T Memory Groupings**

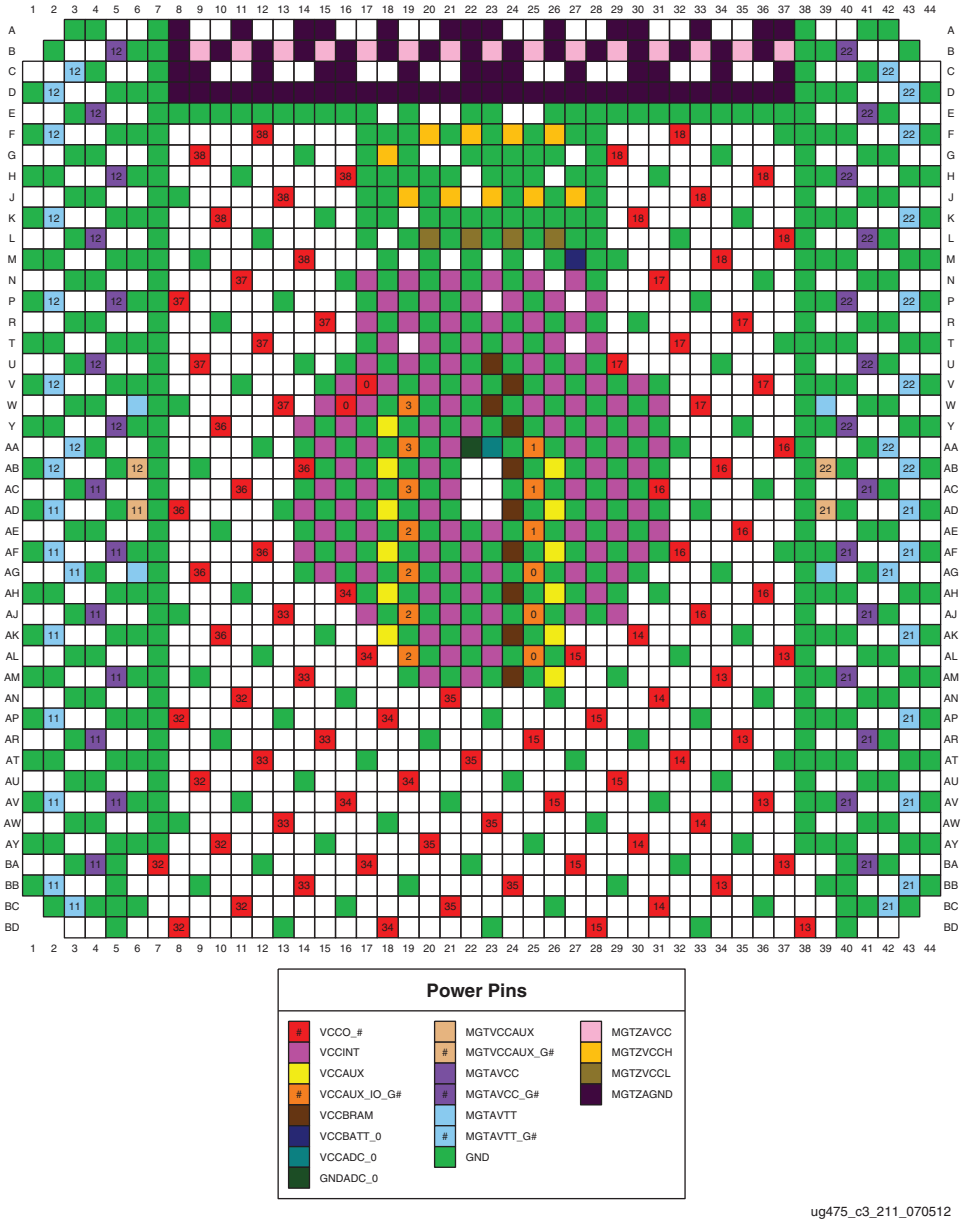
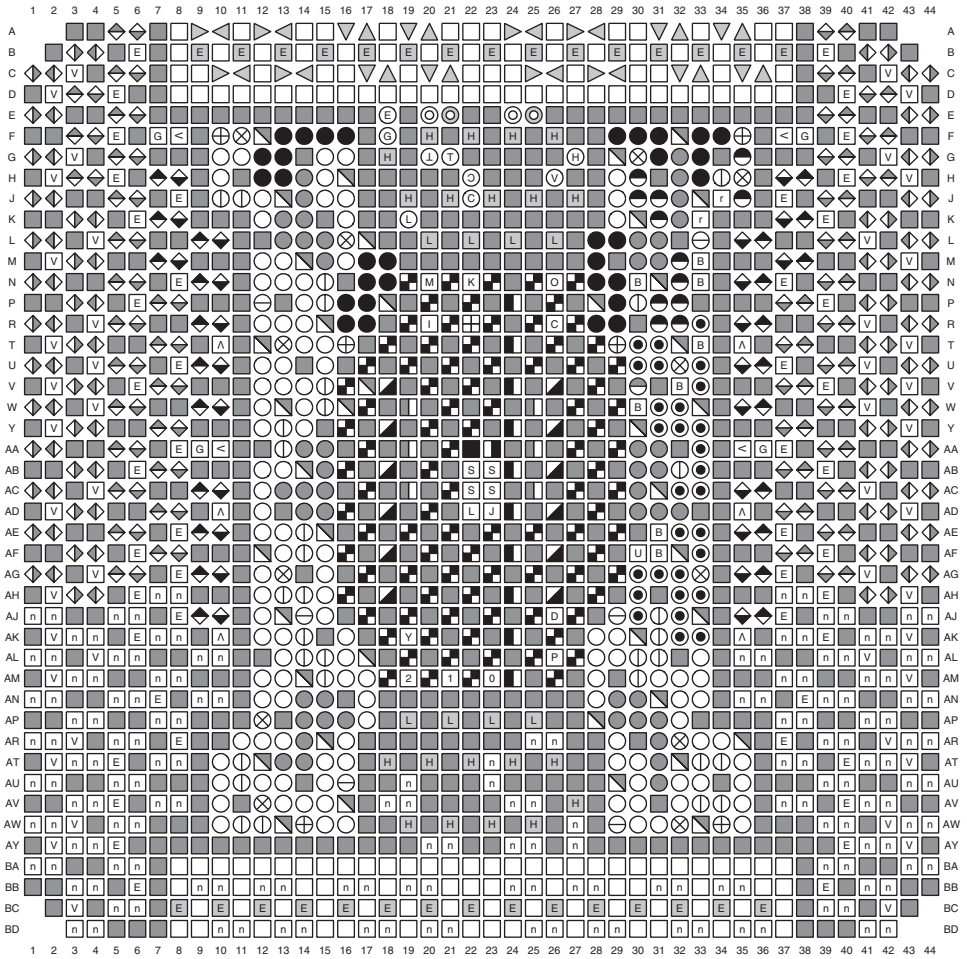


Figure 3-164: **HCG1931 Package—XC7VH580T Power and GND Placement**

HCG1932 Package—XC7VH580T



User I/O Pins	Transceiver Pins		Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	MGTZ_SENSE_AGND	CCLK_0	GND
IO_XX_#	MGTAVTT_G#	MGTZ_SENSE_AVCC	CFGBVS_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	MGTZ_SENSE_VCCH	DONE_0	VCCAUX
ADV_B	MGTAVTTRCAL	MGTZ_SENSE_VCCL	DXP_0	VCCINT
FCS_B	MGTRREF	MGTZ_SENSE_VCC	DXN_0	VCCO_#
FOE_B	MGTREFCLK1/0P	MGTZREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	MGTREFCLK1/0N	MGTZREFCLK1/0N	INIT_B_0	NC
FWE_B	MGTXRXP	MGTZ_THERM_IN	M0_0	
DOUT_CSO_B	MGTXRXN	MGTZ_THERM_OUT	M1_0	
CSI_B	MGTXTXP	MGTZ_OBS_CLK_P	M2_0	
PUDC_B	MGTXTXN	MGTZ_OBS_CLK_N	PROGRAM_B_0	
RDWR_B	MGTHAVCC_G#		TCK_0	
RS0–RS1	MGTHAVTT_G#		TDI_0	
AD0P/AD0N–AD15P/AD15N	MGTHRXP		TDO_0	
EMCCLK	MGTHRXN		TMS_0	
VRN	MGTHTXP		VCCADC_0	
VRP	MGTHTXN		VCCBATT_0	
VREF	MGTZRXP		VP_0	
D00–D31	MGTZRXN		VN_0	
A00–A28	MGTZTXP		VREFP_0	
DQS	MGTZTXN		VREFN_0	
MRCC	MGTZAGND			
SRCC	MGTZAVCC			
	MGTZVCCH			
	MGTZVCCL			

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Figure 3-165: **HCG1932 Package—XC7VH580T Pinout Diagram**

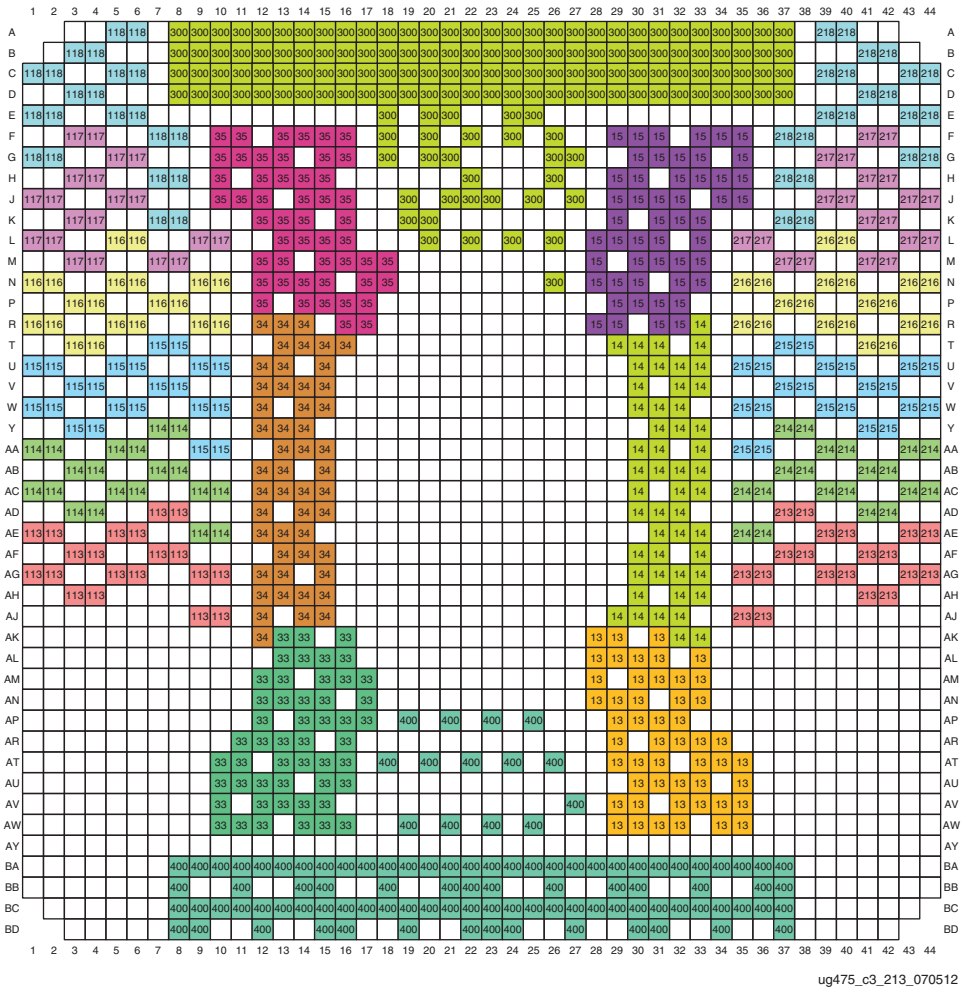


Figure 3-166: **HCG1932 Package—XC7VH580T I/O Banks**

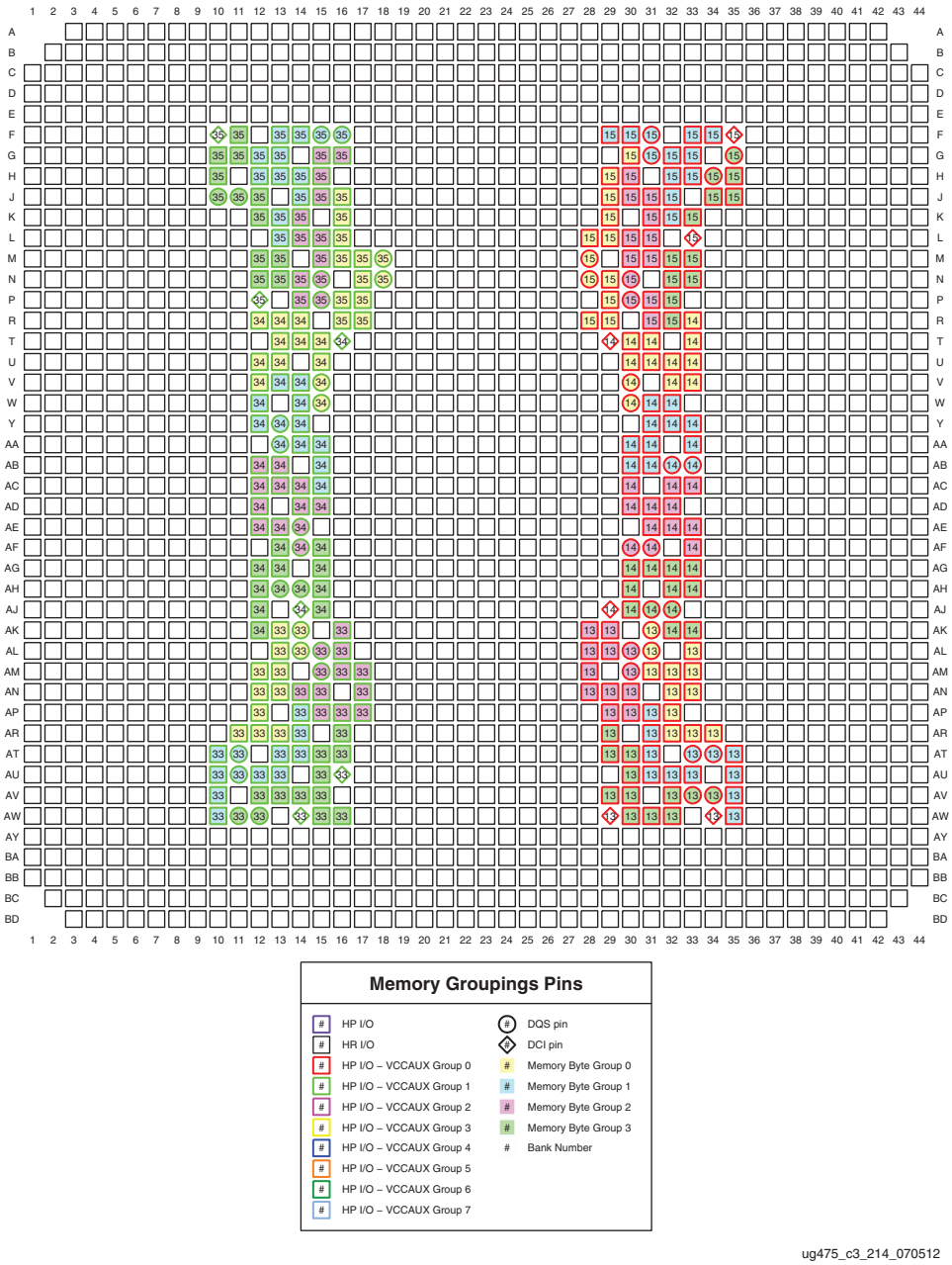


Figure 3-167: **HCG1932 Package—XC7VH580T Memory Groupings**

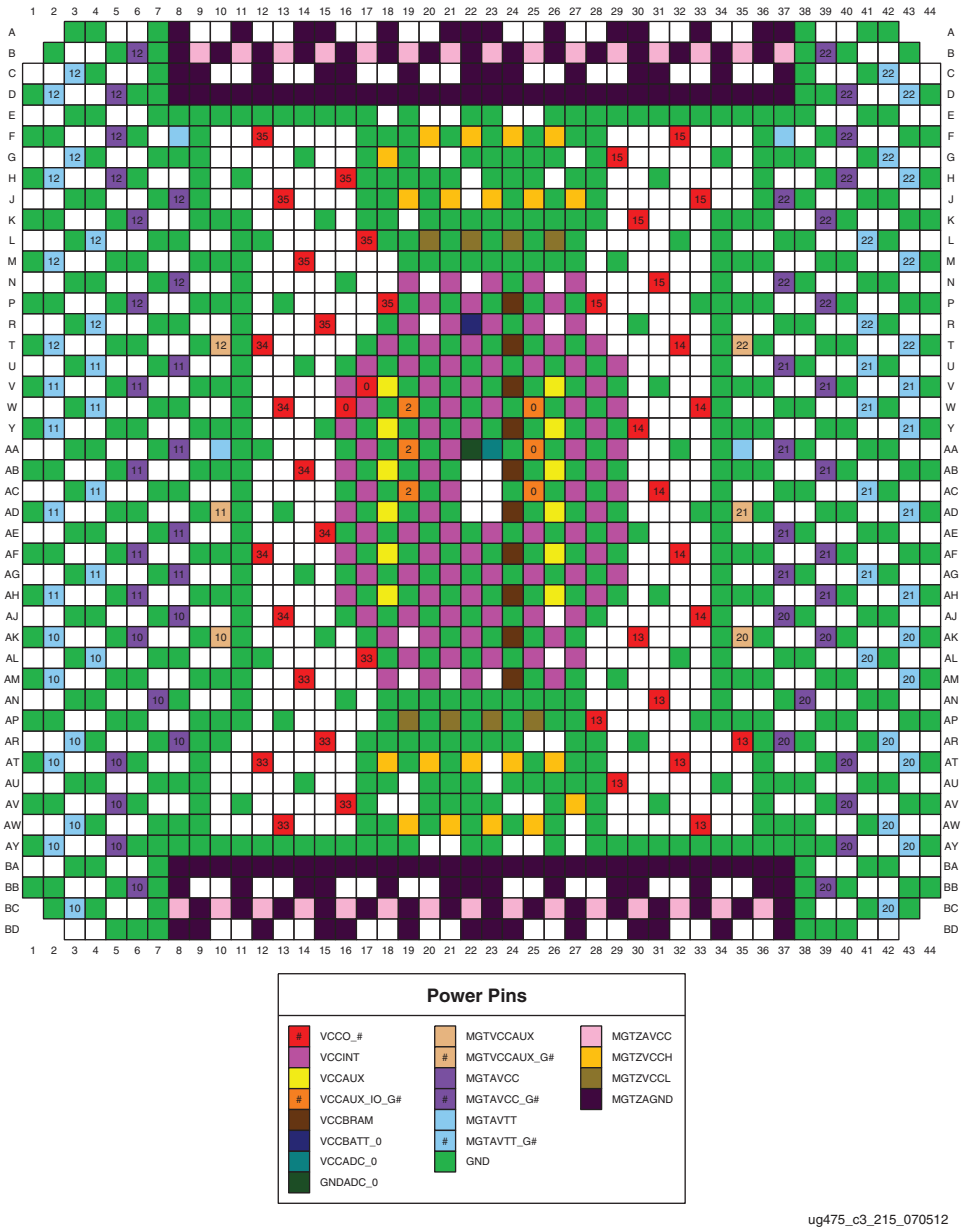


Figure 3-168: **HCG1932 Package—XC7VH580T Power and GND Placement**

HCG1931 Package—XC7VH870T

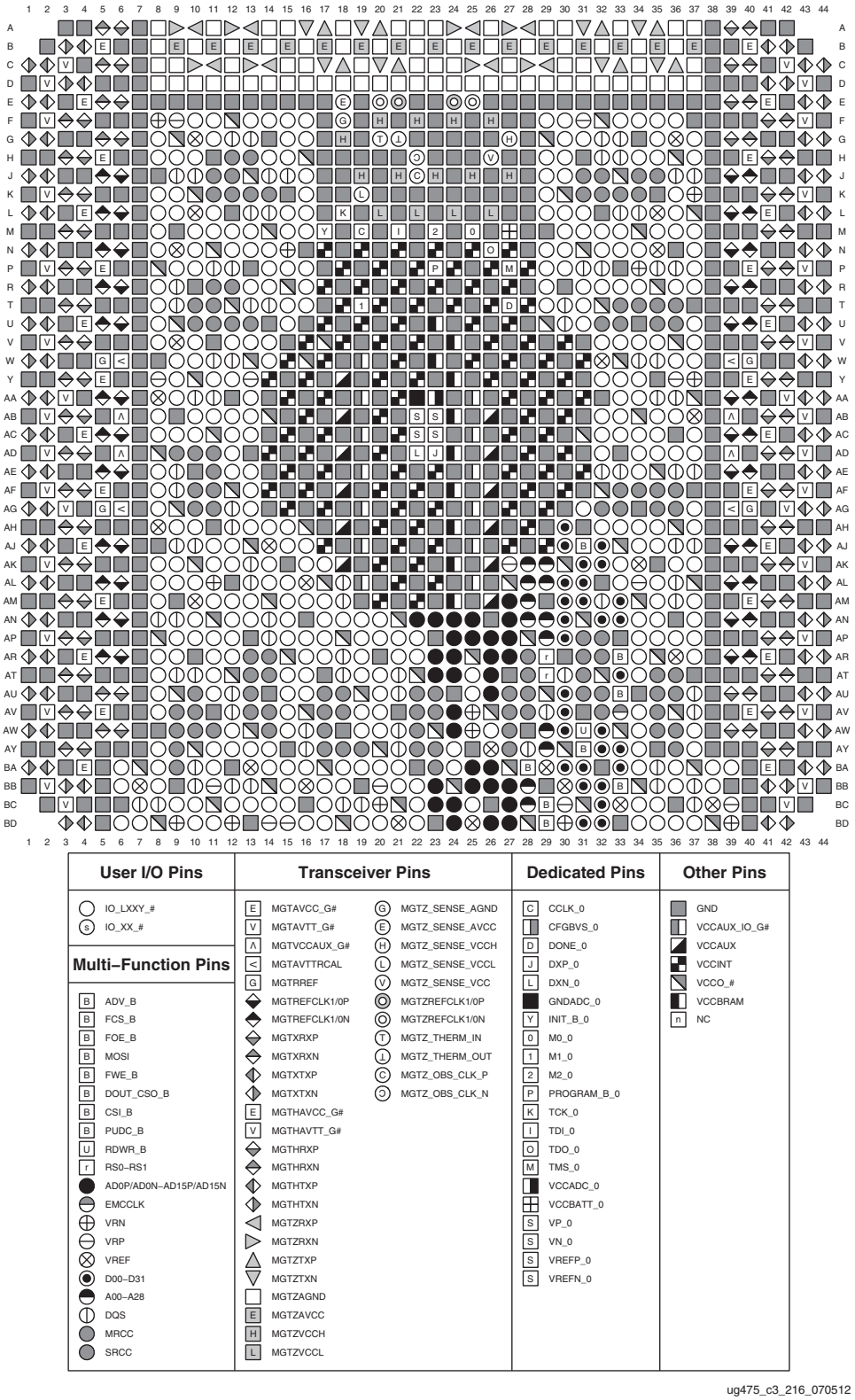


Figure 3-169: **HCG1931 Package—XC7VH870T Pinout Diagram**

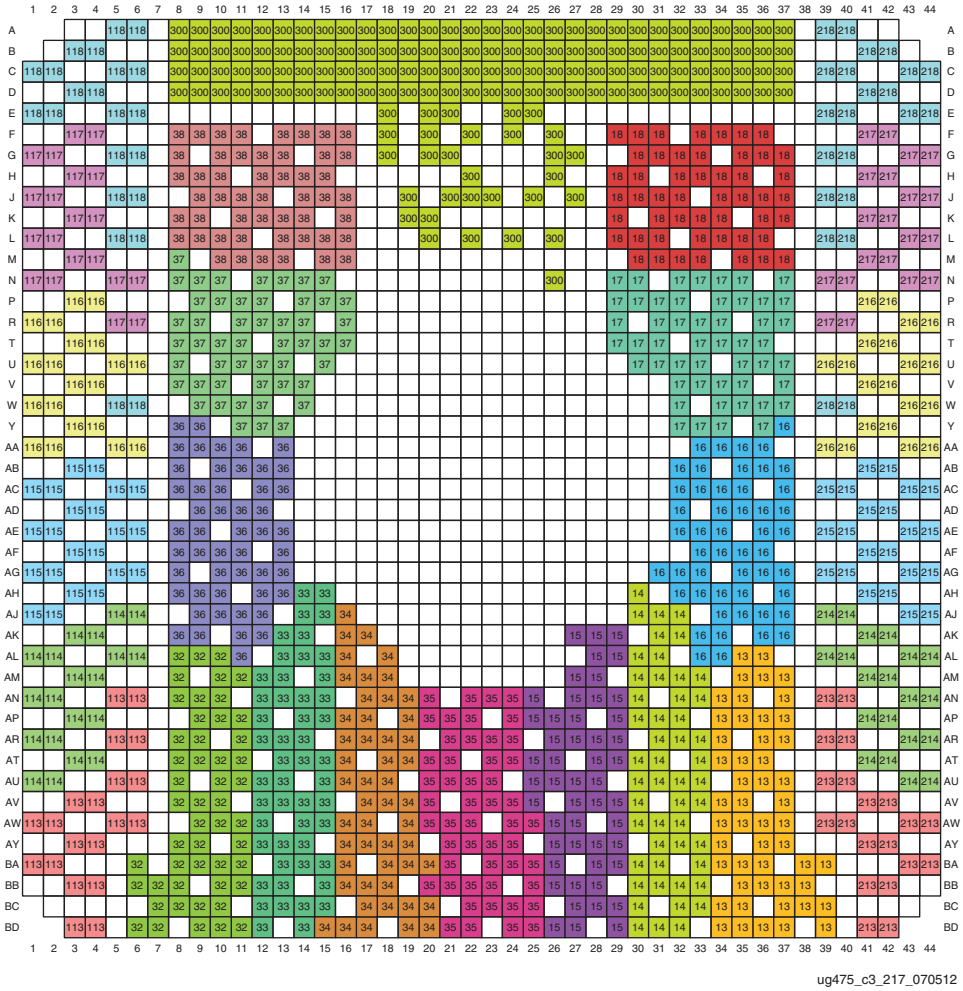


Figure 3-170: **HCG1931 Package—XC7VH870T I/O Banks**

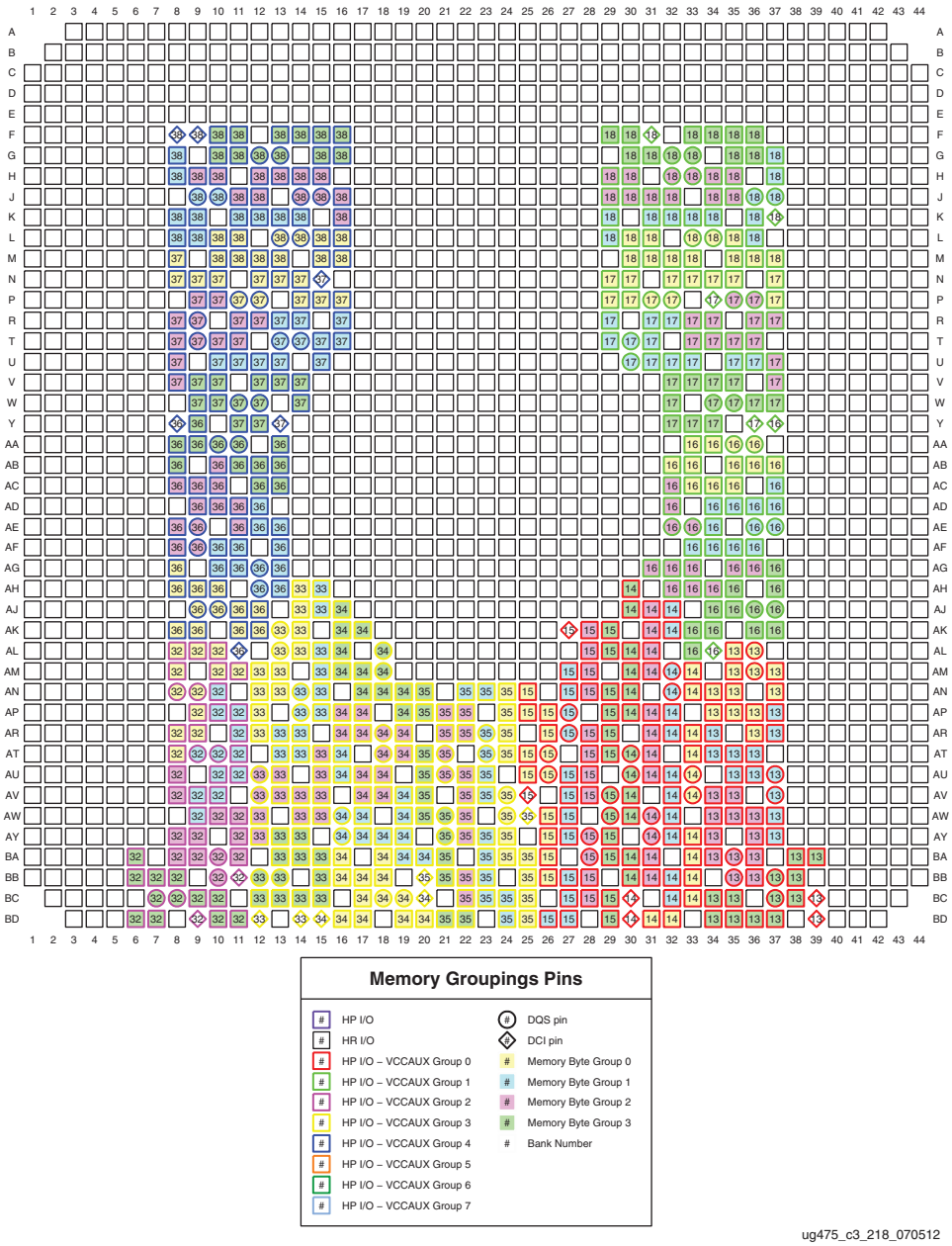


Figure 3-171: **HCG1931 Package—XC7VH870T Memory Groupings**

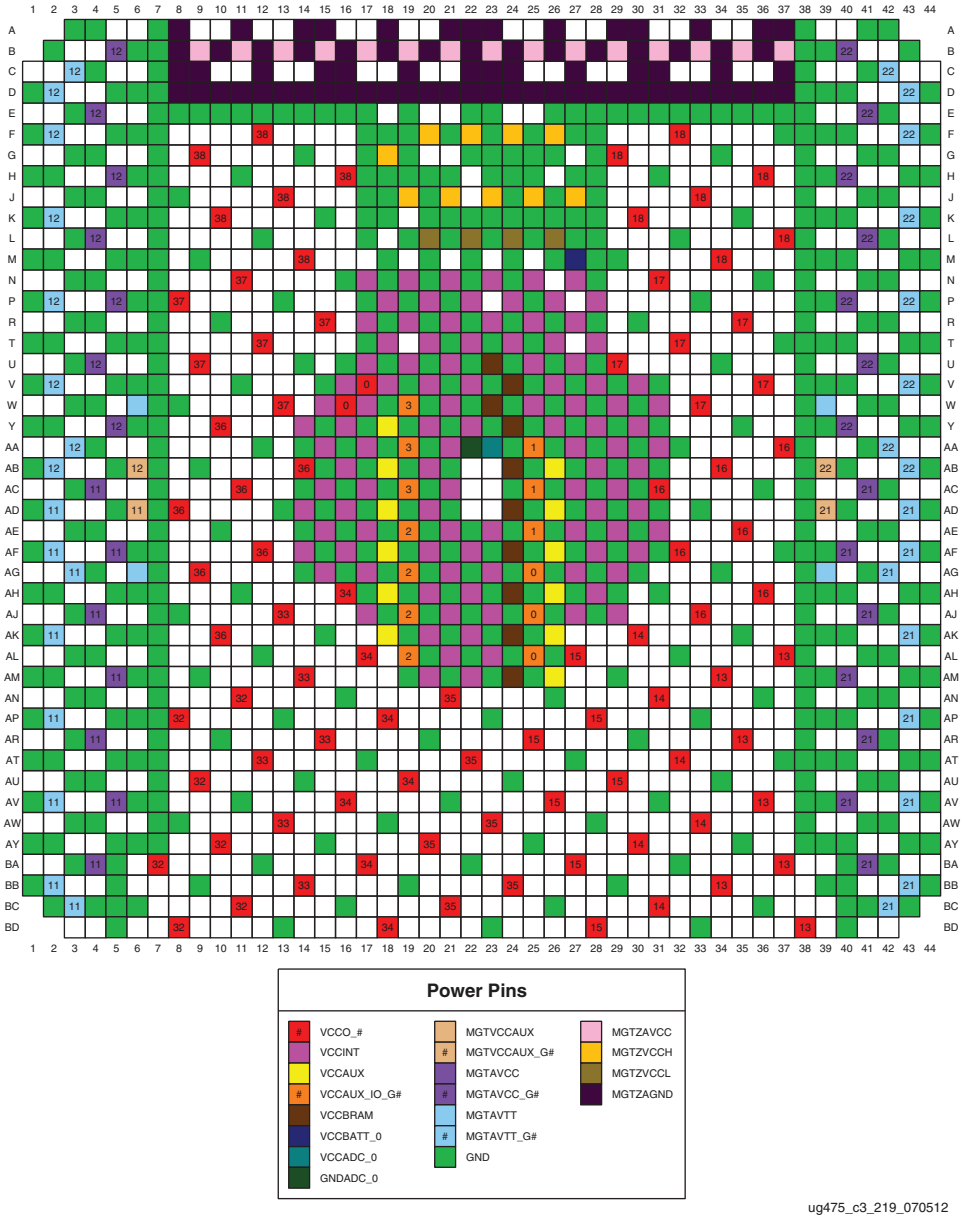
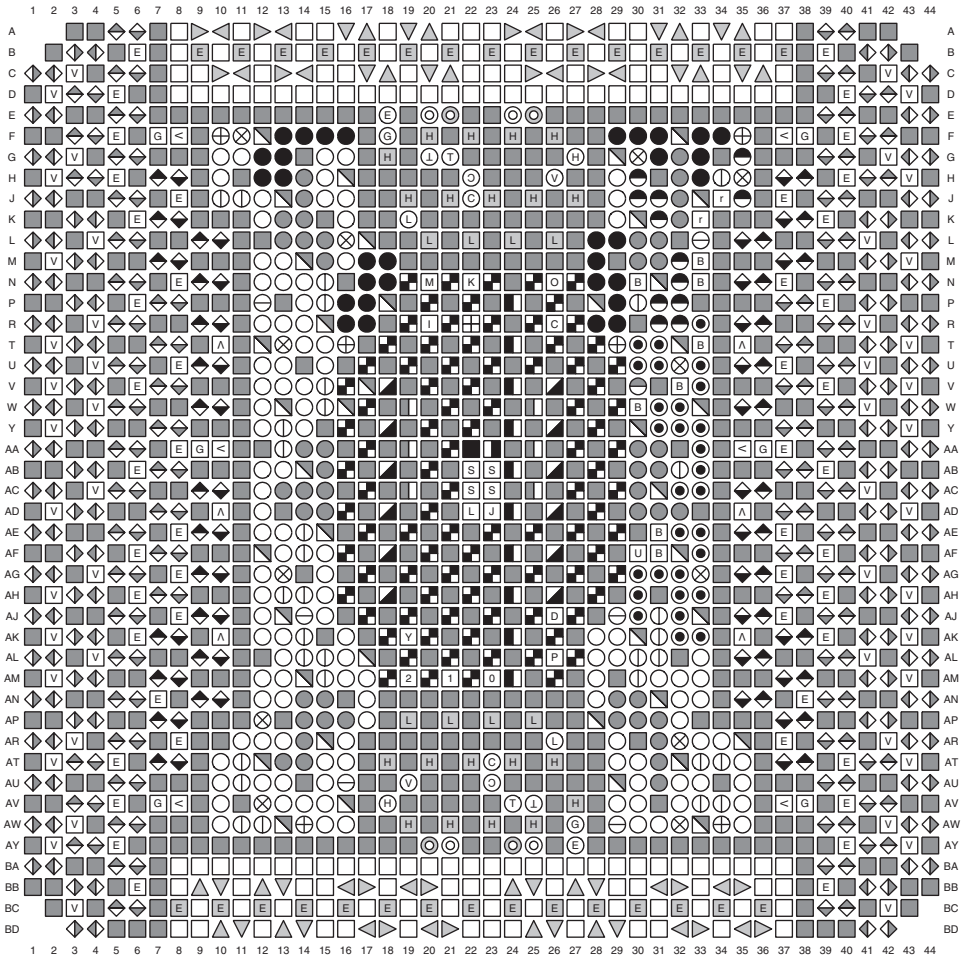


Figure 3-172: **HCG1931 Package—XC7VH870T Power and GND Placement**

HCG1932 Package—XC7VH870T



User I/O Pins	Transceiver Pins		Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	MGTZ_SENSE_AGND	CCLK_0	GND
IO_XX_#	MGTAVTT_G#	MGTZ_SENSE_AVCC	CFGBVS_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	MGTZ_SENSE_VCCH	DONE_0	VCCAUX
ADV_B	MGTAVTTRCAL	MGTZ_SENSE_VCCL	DXP_0	VCCINT
FCS_B	MGTRREF	MGTZ_SENSE_VCC	DXN_0	VCCO_#
FOE_B	MGTREFCLK1/0P	MGTZREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	MGTREFCLK1/0N	MGTZREFCLK1/0N	INIT_B_0	NC
FWE_B	MGTXRXP	MGTZ_THERM_IN	M0_0	
DOUT_CSO_B	MGTXRXN	MGTZ_THERM_OUT	M1_0	
CSI_B	MGTXTXP	MGTZ_OBS_CLK_P	M2_0	
PUDC_B	MGTXTXN	MGTZ_OBS_CLK_N	PROGRAM_B_0	
RDWR_B	MGTHAVCC_G#		TCK_0	
RS0–RS1	MGTHAVTT_G#		TDI_0	
AD0P/AD0N–AD15P/AD15N	MGTHRXP		TDO_0	
EMCCLK	MGTHRXN		TMS_0	
VRN	MGTHTXP		VCCADC_0	
VRP	MGTHTXN		VCCBATT_0	
VREF	MGTZRXP		VP_0	
D00–D31	MGTZRXN		VN_0	
A00–A28	MGTZTXP		VREFP_0	
DQS	MGTZTXN		VREFN_0	
MRCC	MGTZAGND			
SRCC	MGTZAVCC			
	MGTZVCCH			
	MGTZVCCL			

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Figure 3-173: **HCG1932 Package—XC7VH870T Pinout Diagram**

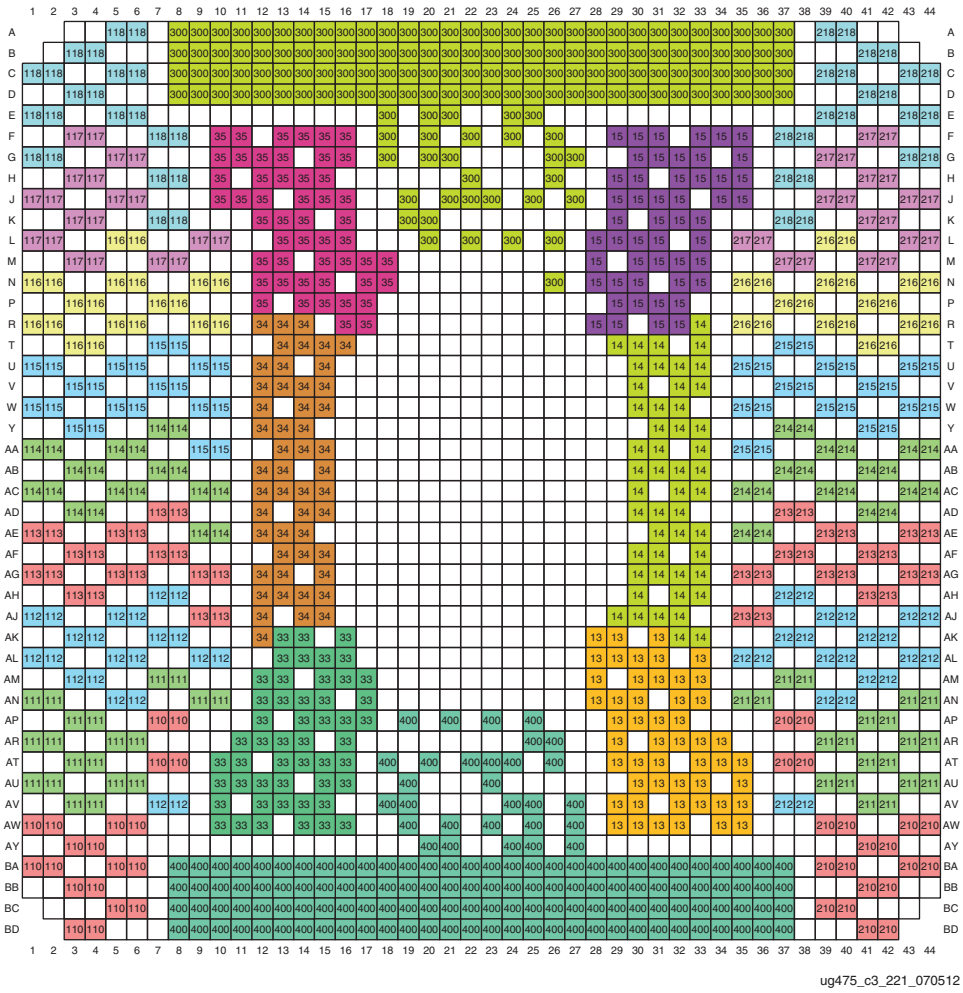


Figure 3-174: **HCG1932 Package—XC7VH870T I/O Banks**

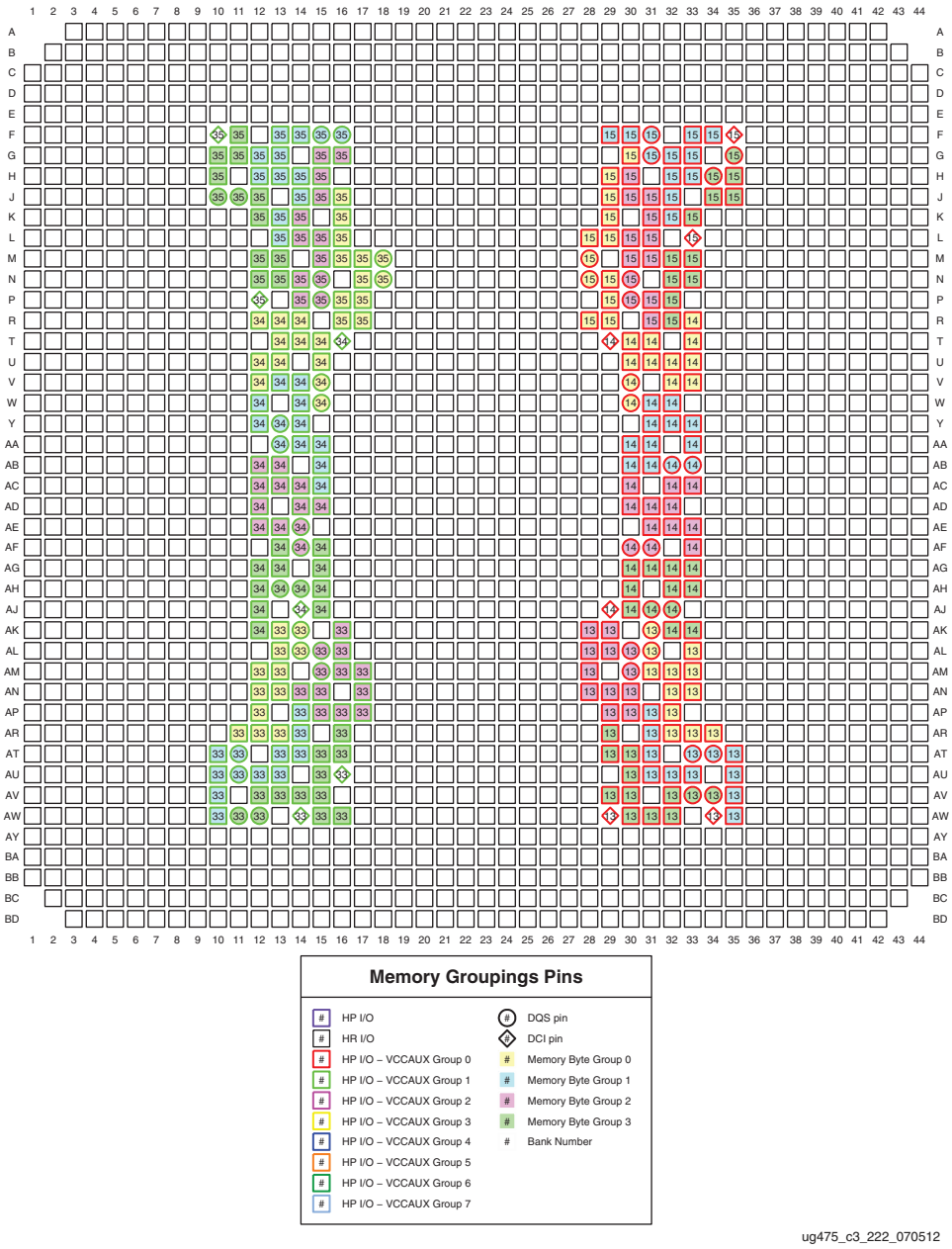


Figure 3-175: **HCG1932 Package—XC7VH870T Memory Groupings**

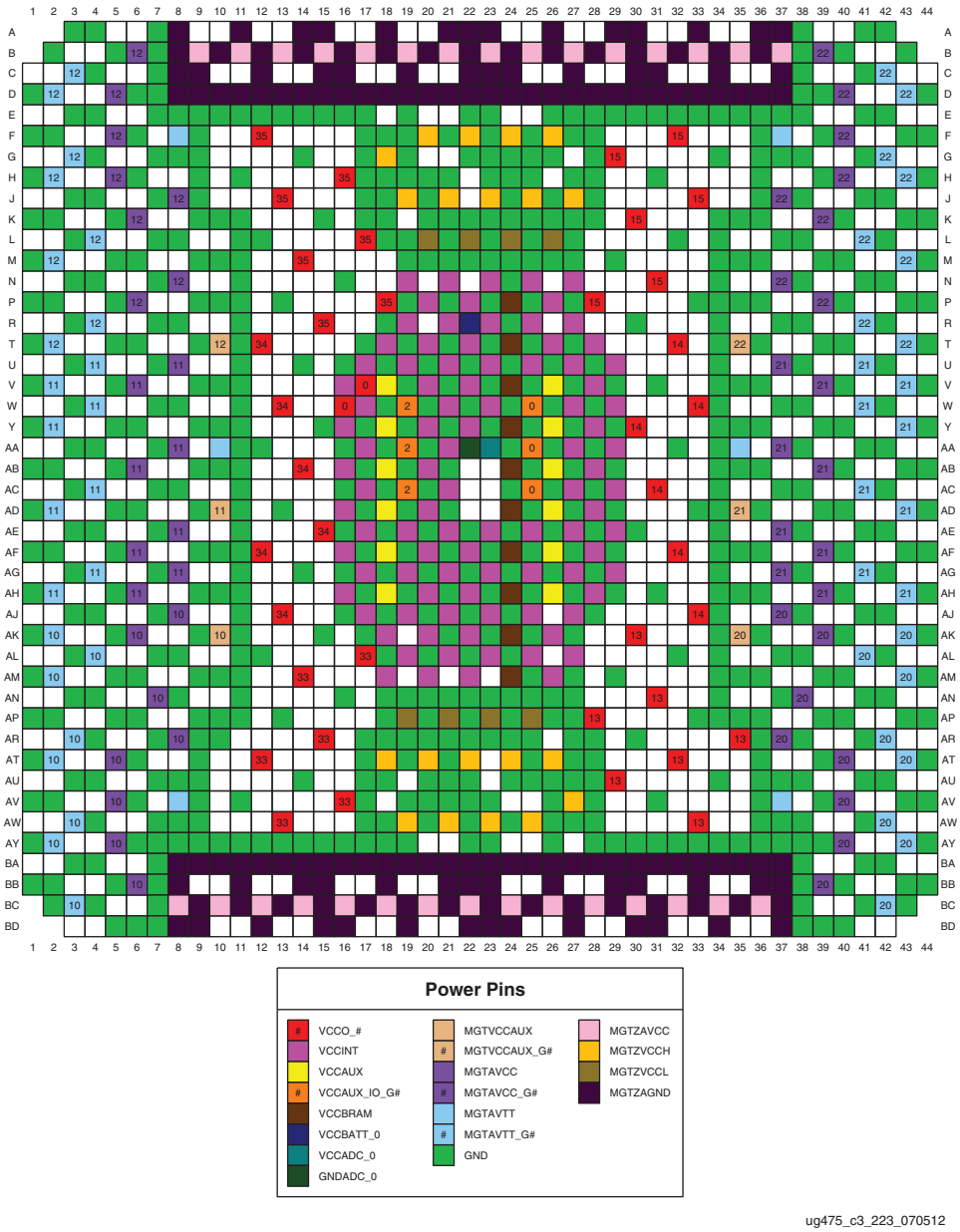


Figure 3-176: **HCG1932 Package—XC7VH870T Power and GND Placement**

XILINX®

Chapter 4

Mechanical Drawings

Summary

This chapter provides mechanical drawings (package specifications) of the following 7 series FPGA packages.

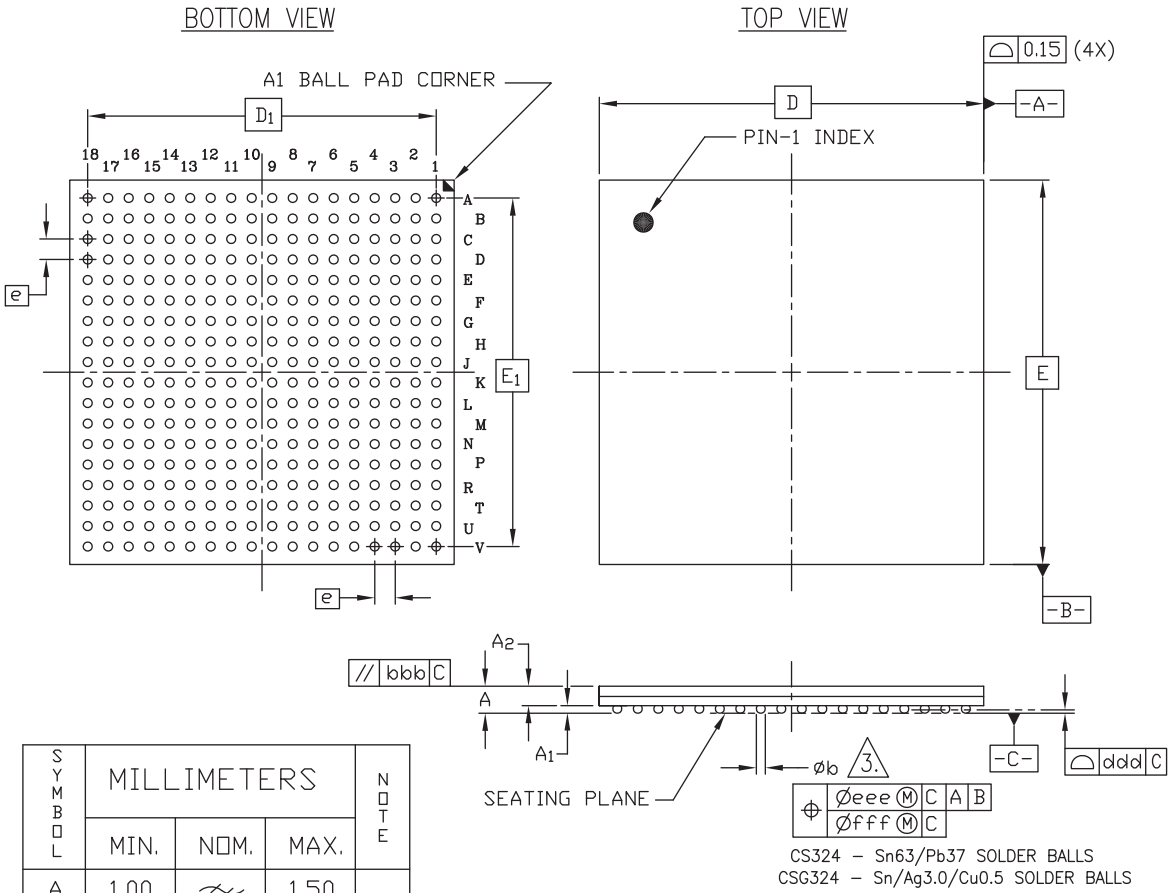
Artix-7 FPGAs

Kintex-7 FPGAs

Virtex-7 FPGAs

Note: This chapter is intentionally missing drawings.

CS/CSG324 Wire-Bond Chip-Scale BGA (Artix-7 FPGAs) (0.8 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.00		1.50	
A_1	0.25	0.30	0.40	
A_2	0.75	0.90	1.10	
D/E	15.00 BSC			
D_1/E_1	13.60 BSC			
e	0.80 BSC			
øb	0.35	0.40	0.45	3
bbb			0.20	
ddd			0.10	
eee			0.15	
fff			0.08	
M	18			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. CONFORMS TO JEDEC MO–275–KKAC–1.

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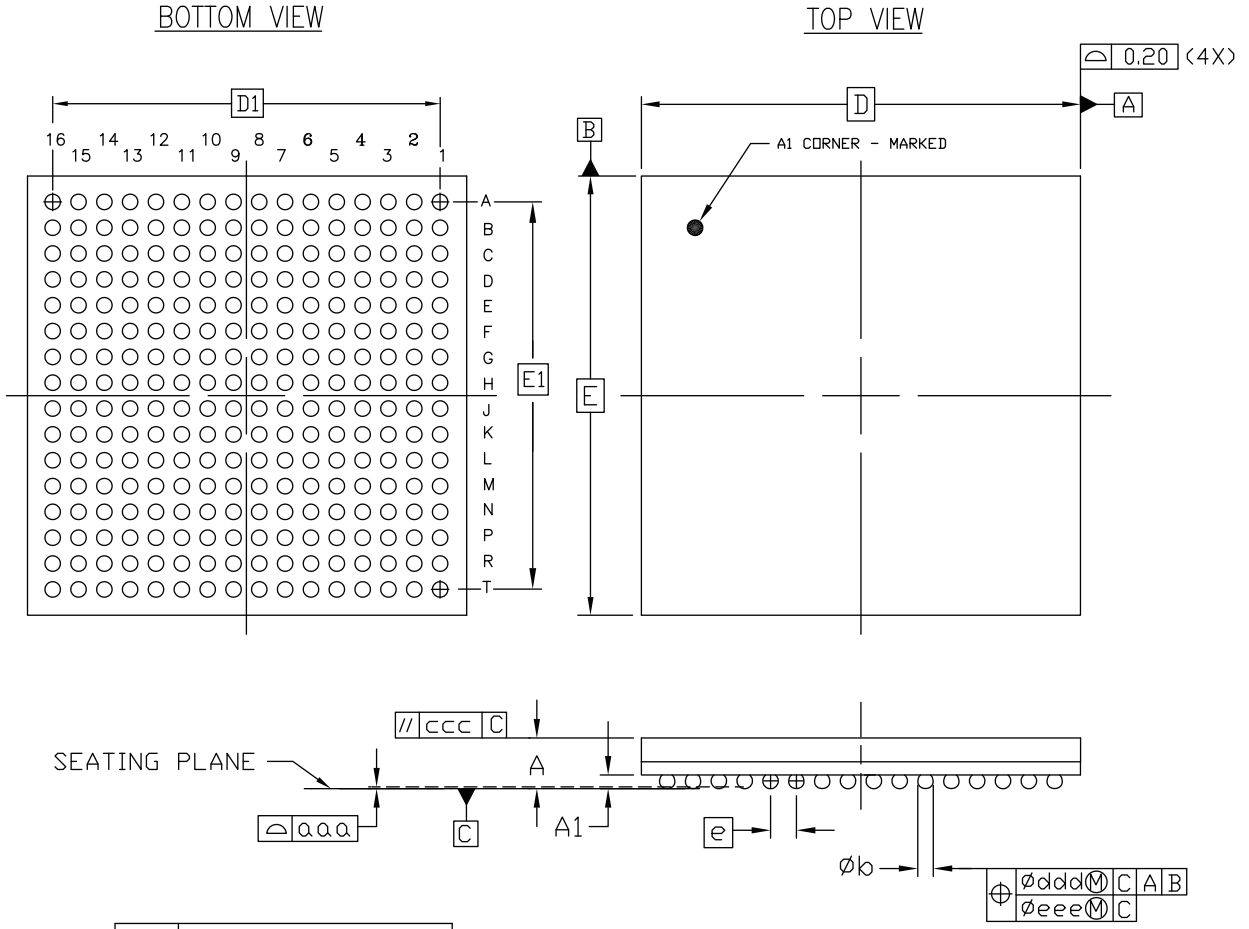
Figure 4-1: **CS/CSG324 Wire-Bond Chip-Scale BGA Package Specifications for Artix-7 FPGAs**

FTG256 Wire-Bond Fine-Pitch Thin BGA (Artix-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		1.40	1.55
A_1	0.30	0.40	0.50
D/E	17.00 BSC		
D_1/E_1	15.00 REF		
e	1.00 BSC		
øb	0.40	0.50	0.60
aaa			0.15
ccc			0.15
ddd			0.25
eee			0.10
M	16		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 AAF–1 EXCEPT FOR THE SOLDER BALL SIZE.

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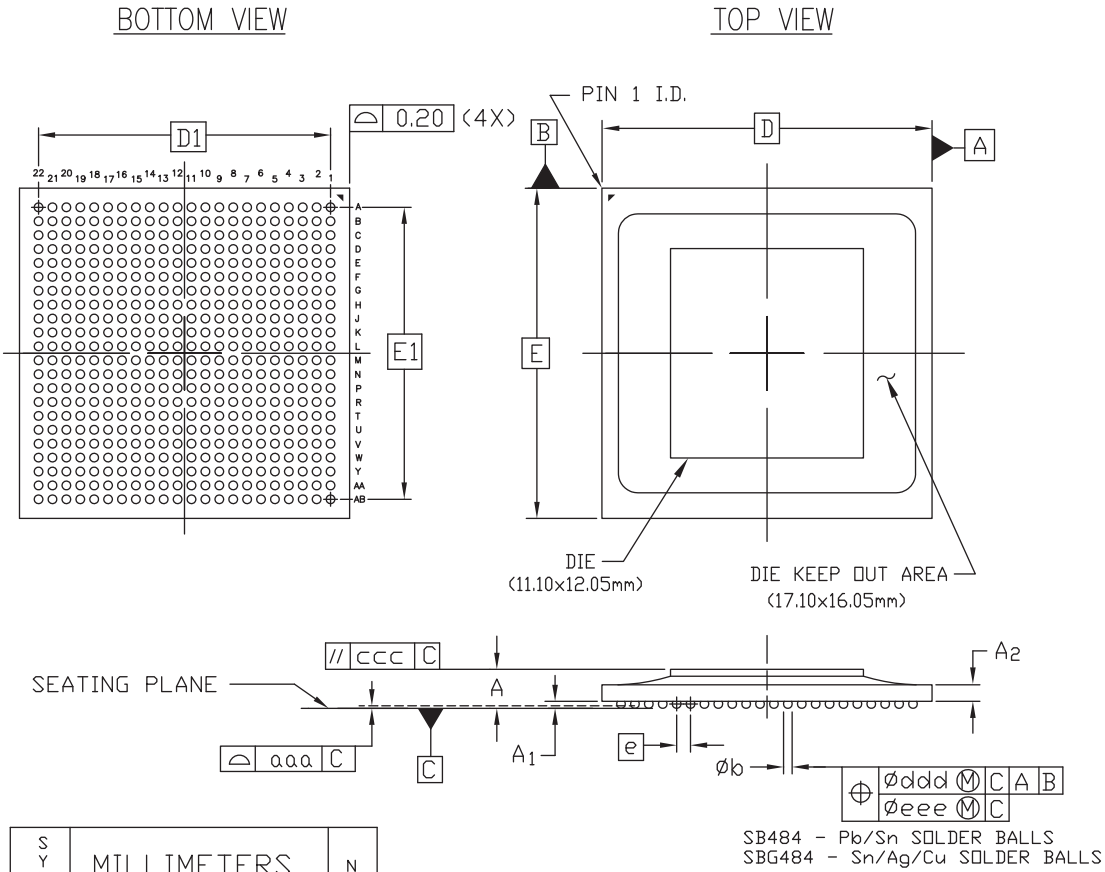
Figure 4-2: **FTG256 Wire-Bond Fine-Pitch Thin BGA Package Specifications for Artix-7 FPGAs**

SBG484 Flip-Chip Lidless BGA (Artix-7 FPGAs) (0.8 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.04	2.24	2.44	
A_1	0.36	0.40	0.44	
A_2	0.88	0.98	1.08	
D/E	19.00 BASIC			
D_1/E_1	16.80 REF			
e	0.80 BASIC			
øb	0.45	0.50	0.55	
aaa	~	~	0.20	
ccc	~	~	0.20	
ddd	~	~	0.15	
eee	~	~	0.08	
M	22			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MO–275–PPA2 EXCEPT DIM "A"

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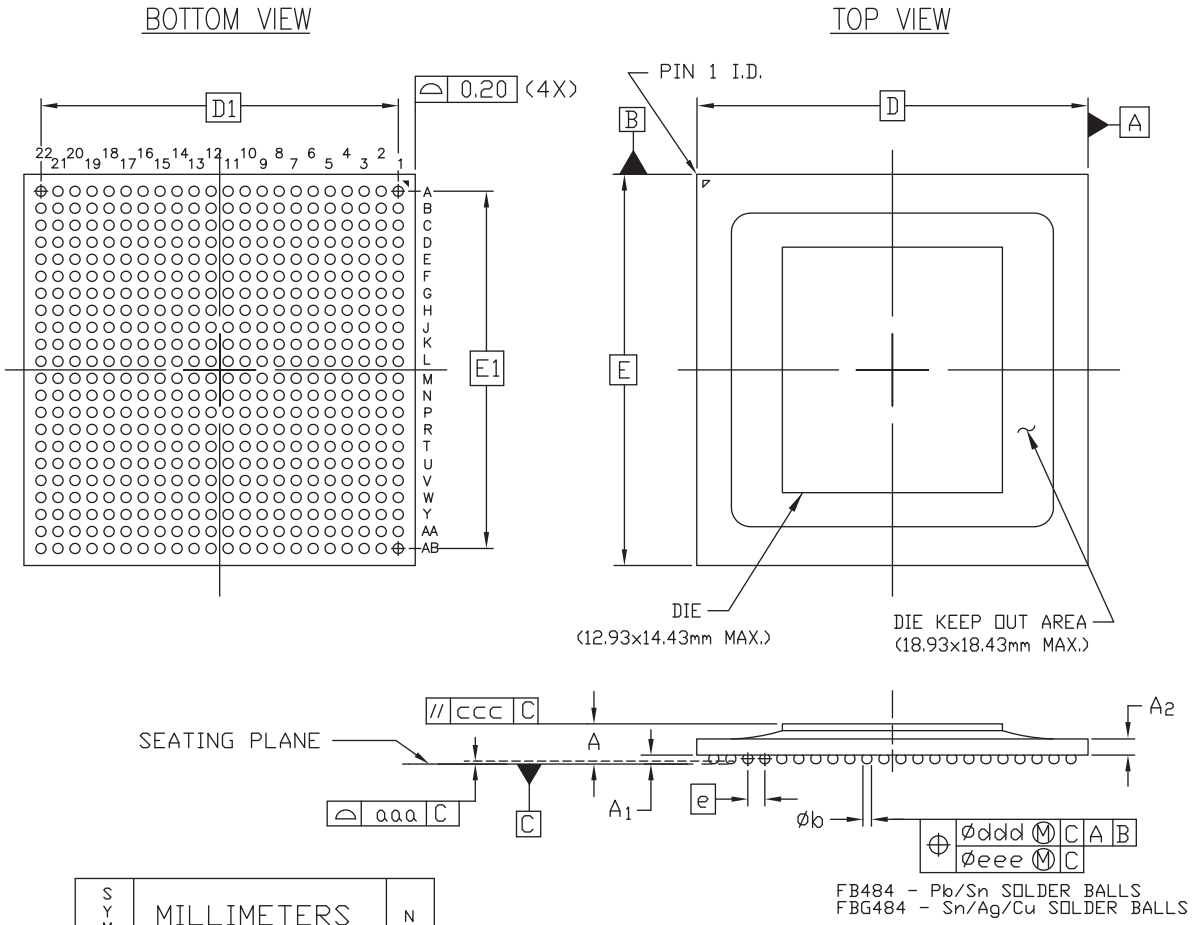
Figure 4-3: **SBG484 Flip-Chip Lidless BGA Package Specifications for Artix-7 FPGAs**

FB/FBG484 Flip-Chip Lidless BGA (Artix-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.14	2.34	2.54	
A_1	0.40	0.50	0.60	
A_2	0.83	0.98	1.13	
D/E	23.00 BASIC			
D_1/E_1	21.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.25	
ddd			0.25	
eee			0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034
4. SEE FOLLOWING PAGES FOR SPECIFIC DIE SIZE PER DEVICE

ug475_c4_xx_070912

Figure 4-4: **FB/FBG484 Flip-Chip Lidless BGA Package Specifications for Artix-7 FPGAs**

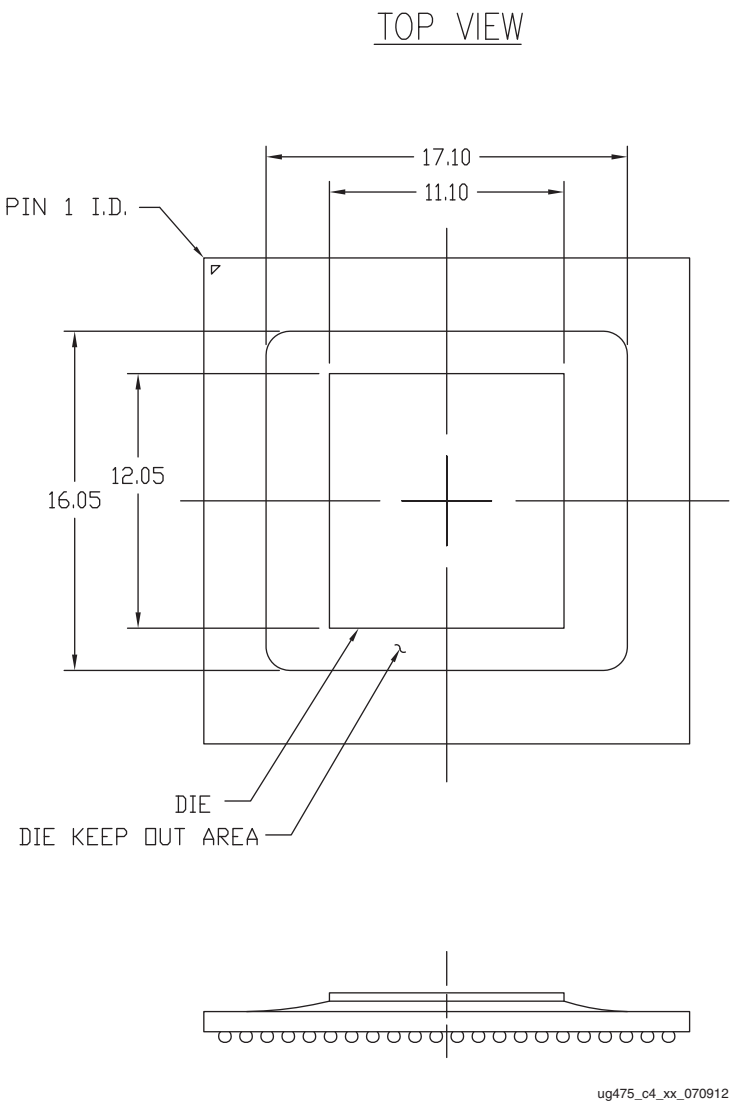
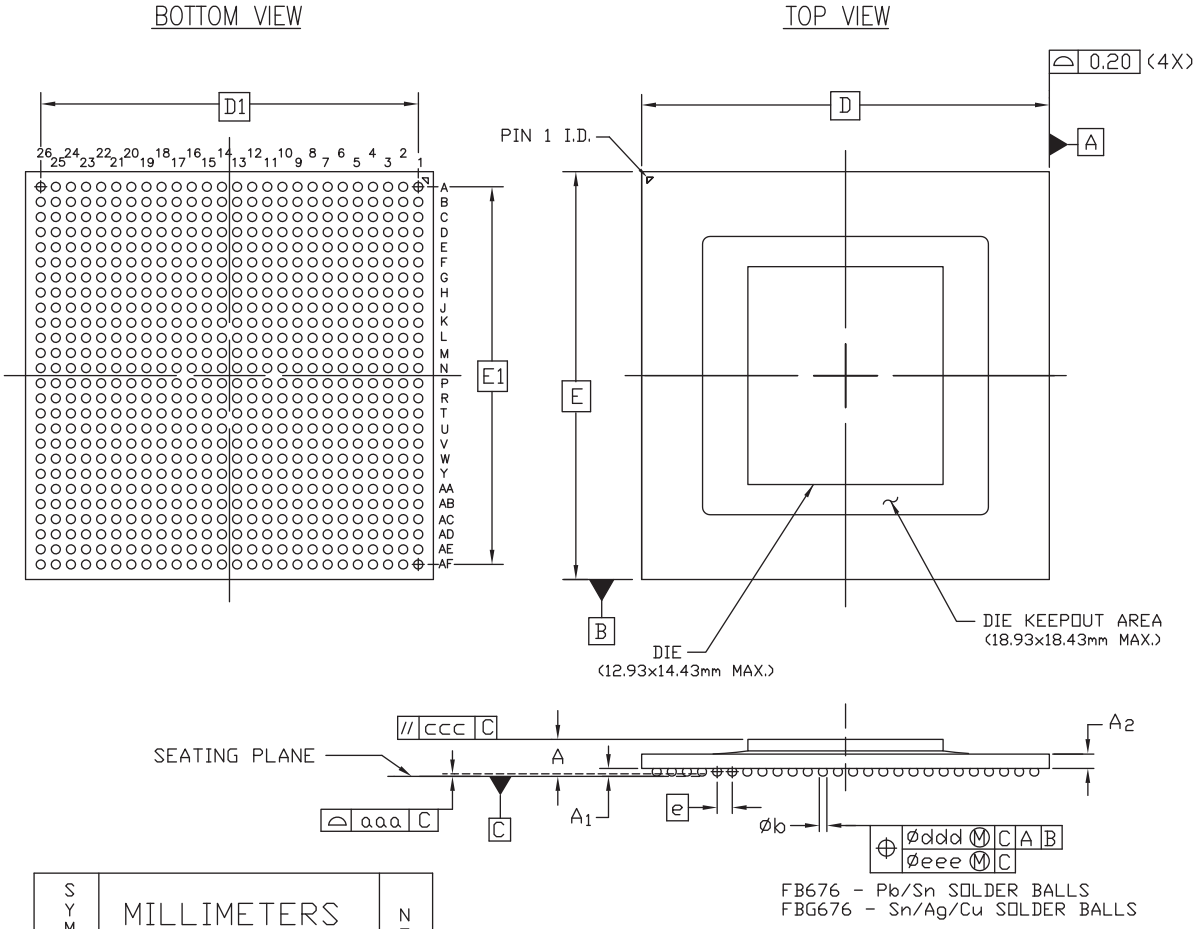


Figure 4-5: **XC7A200T FB/FBG484 Die Dimensions**

FB/FBG676 Flip-Chip Lidless BGA (Artix-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.14	2.34	2.54	
A_1	0.40	0.50	0.60	
A_2	0.88	0.98	1.08	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034
4. SEE FOLLOWING PAGES FOR SPECIFIC DIE SIZE PER DEVICE

ug475_c4_106_070912

Figure 4-6: **FB/FBG676 Flip-Chip Lidless BGA Package Specifications for Artix-7 FPGAs**

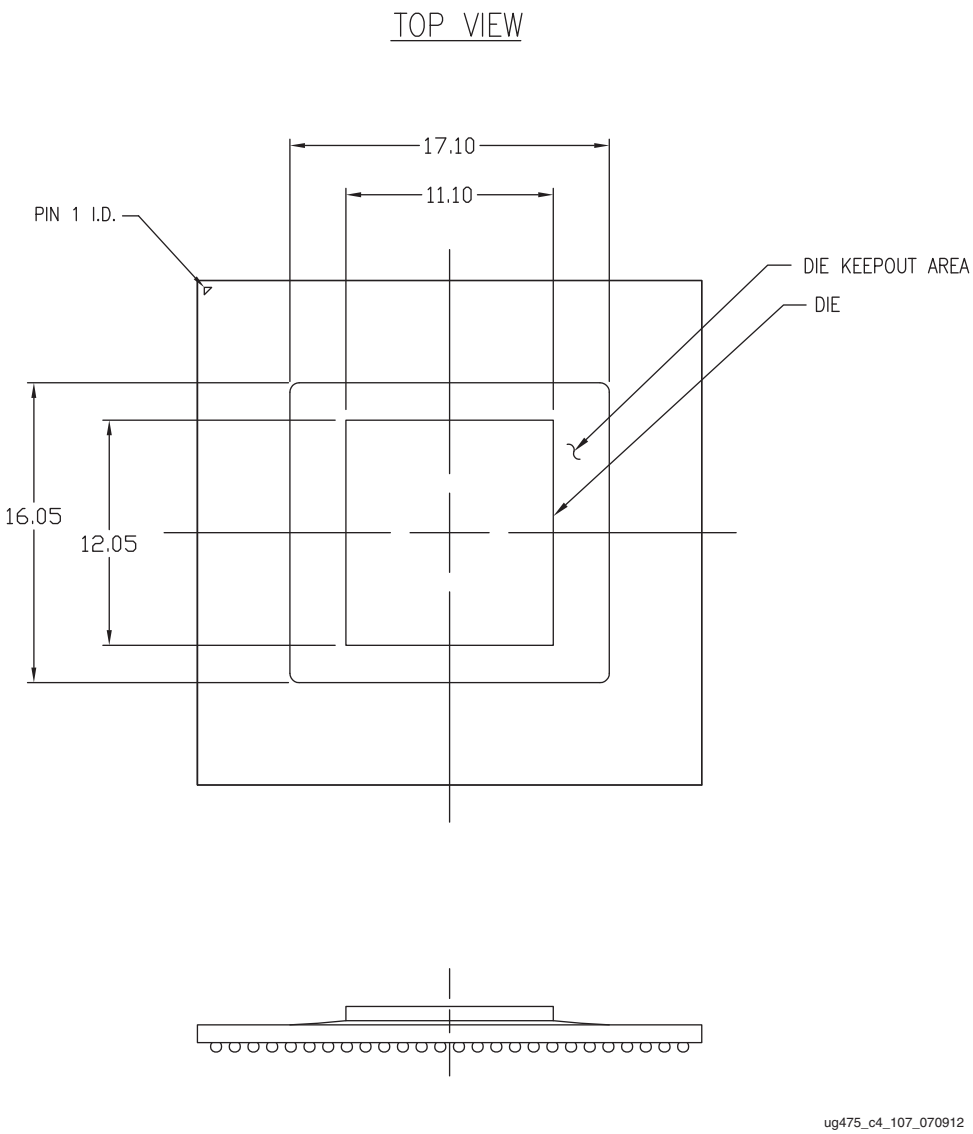
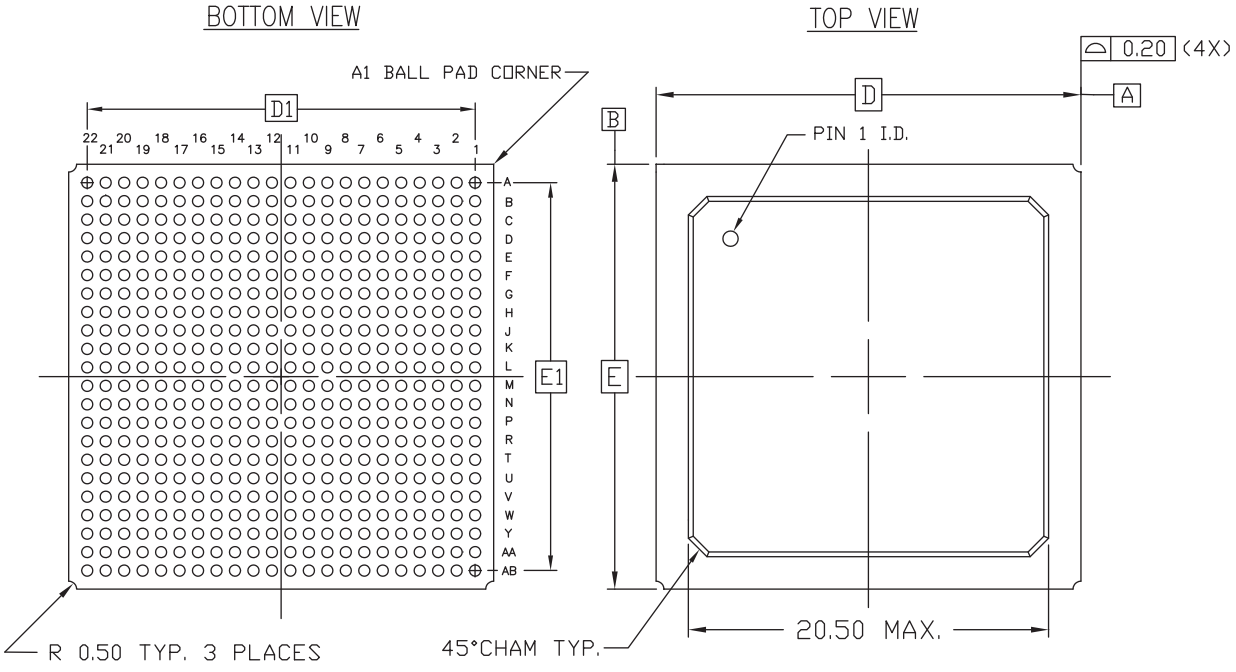


Figure 4-7: **XC7A200T FB/FBG676 Die Dimensions**

FG/FGG484 Wire-Bond Fine-Pitch BGA (Artix-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.00	2.20	2.60	
A_1	0.35	0.50	0.60	
D/E	23.00 BSC			
D_1/E_1	21.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	22			2

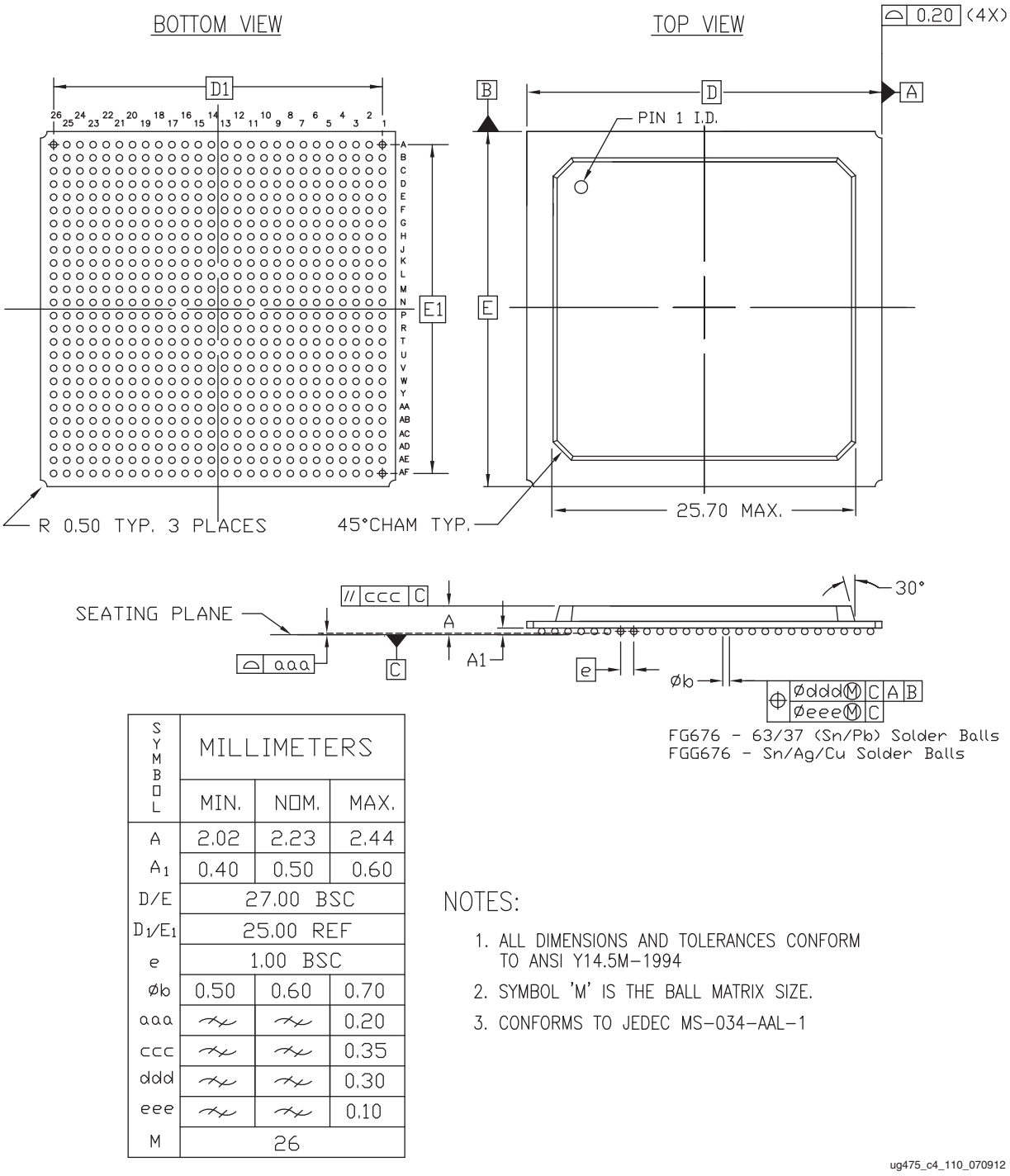
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAJ–1.

ug475_c4_109_071212

Figure 4-8: **FG/FGG484 Wire-bond Fine-Pitch BGA Package Specification for Artix-7 FPGAs**

FG/FGG676 Wire-Bond Fine-Pitch BGA (Artix-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.02	2.23	2.44
A_1	0.40	0.50	0.60
D/E	27.00 BSC		
D_1/E_1	25.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.10
M	26		

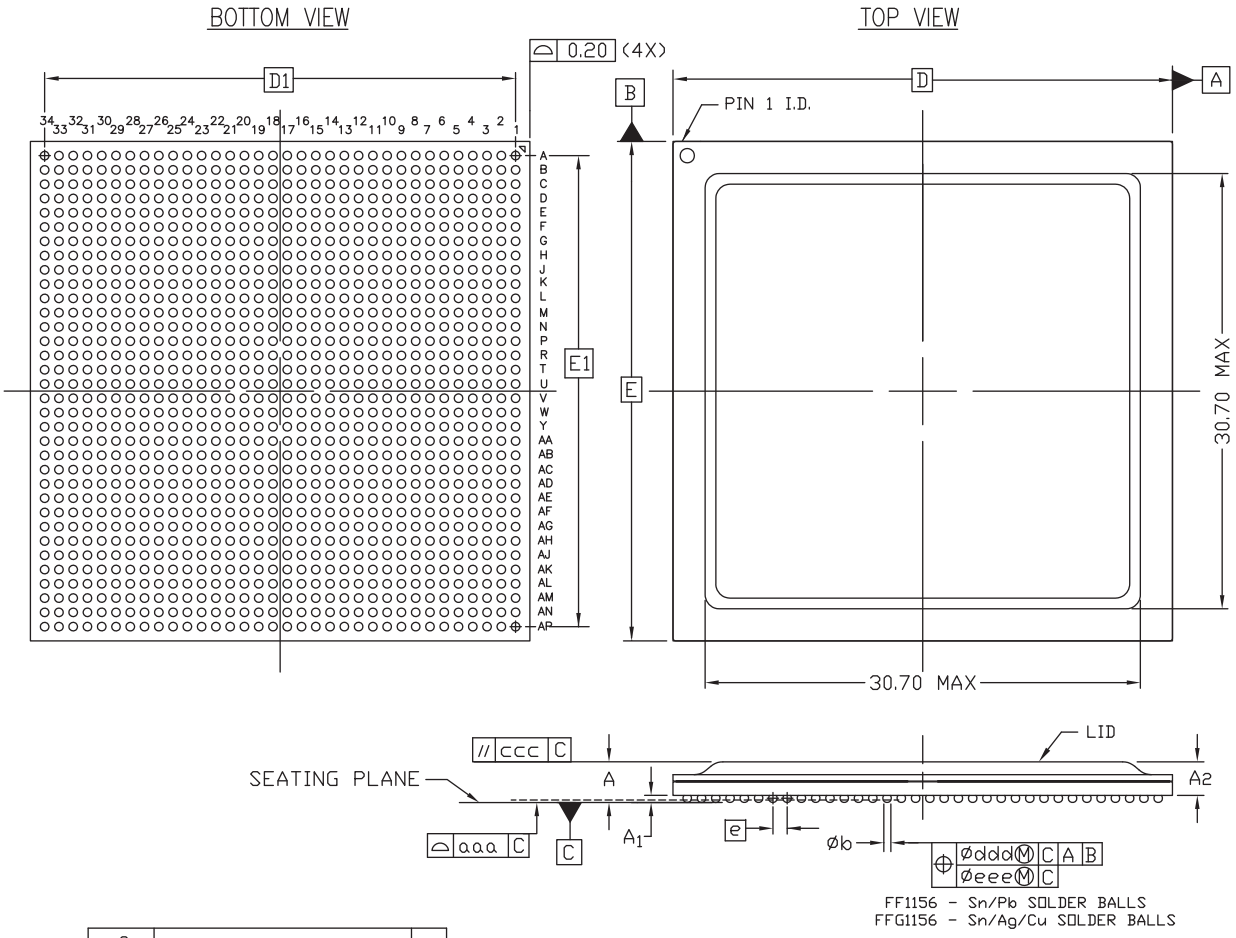
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1

ug475_c4_110_070912

Figure 4-9: **FG/FGG676 Wire-bond Fine-Pitch BGA Package Specification for Artix-7 FPGAs**

FF/FFG1156 Flip-Chip BGA (Artix-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.55	~	3.15	
A_1	0.40	0.50	0.60	
A_2	2.15	~	2.55	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	4
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	34			2

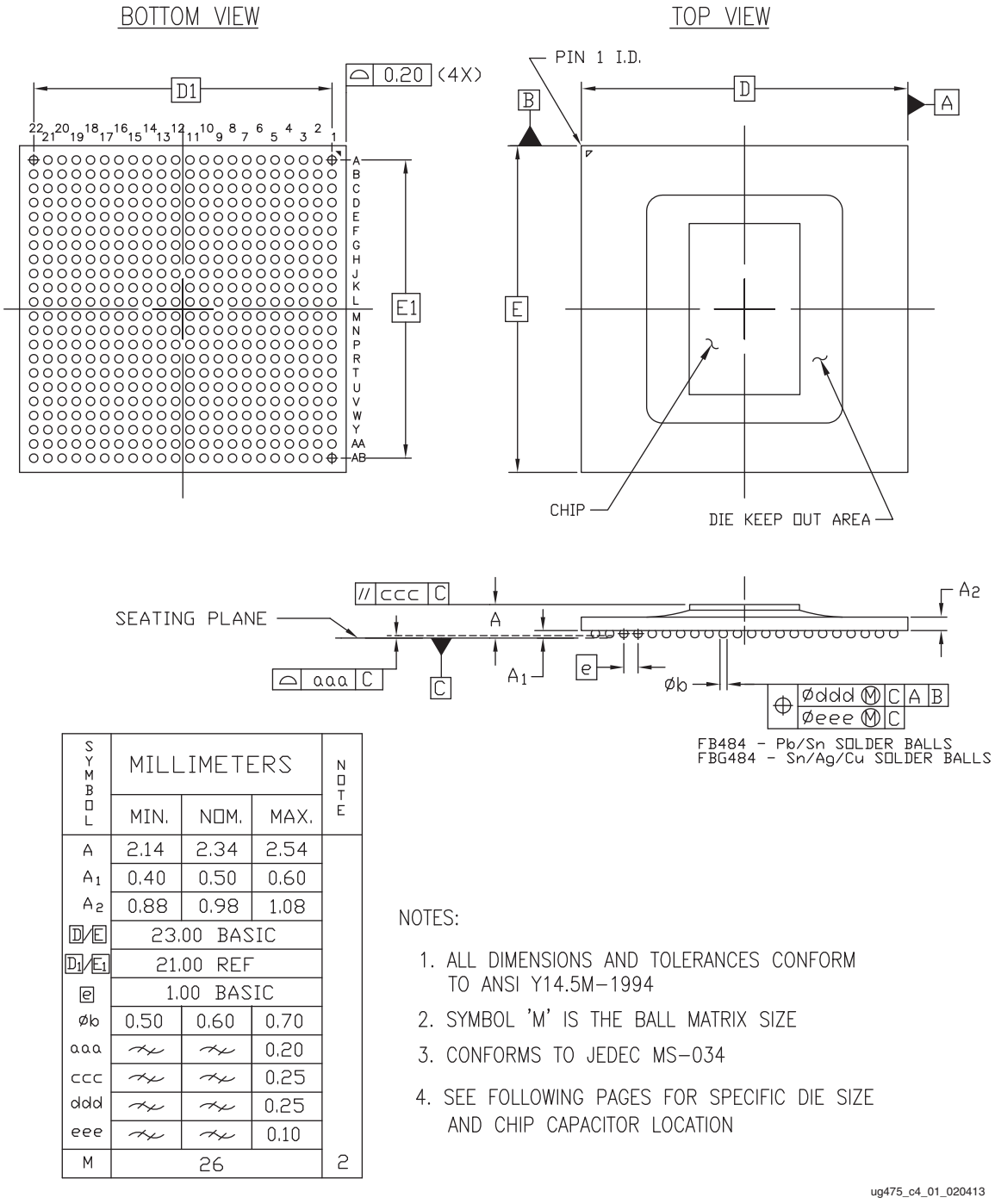
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAR–1
4. ACTUAL SOLDER BALL COUNT = 1156
5. THIS PACKAGE IS USED FOR ARTIX®–7 FPGAs REFER TO PK384 FOR THE MECHANICAL DRAWING OF FF1156 PACKAGE USED FOR VIRTEX®–5 FPGAS AND PK401 FOR VIRTEX®–6 FPGAS

ug475_c4_111_020813

Figure 4-10: **FF/FFG1156 Flip-Chip BGA Package Specification for Artix-7 FPGAs**

FB/FBG484 Flip-Chip Lidless BGA (Kintex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.14	2.34	2.54	
A_1	0.40	0.50	0.60	
A_2	0.88	0.98	1.08	
D/E	23.00 BASIC			
D_1/E_1	21.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.25	
ddd			0.25	
eee			0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034
4. SEE FOLLOWING PAGES FOR SPECIFIC DIE SIZE AND CHIP CAPACITOR LOCATION

ug475_c4_01_020413

Figure 4-11: **FB/FBG484 Flip-Chip Lidless BGA Package Specifications for Kintex-7 FPGAs**

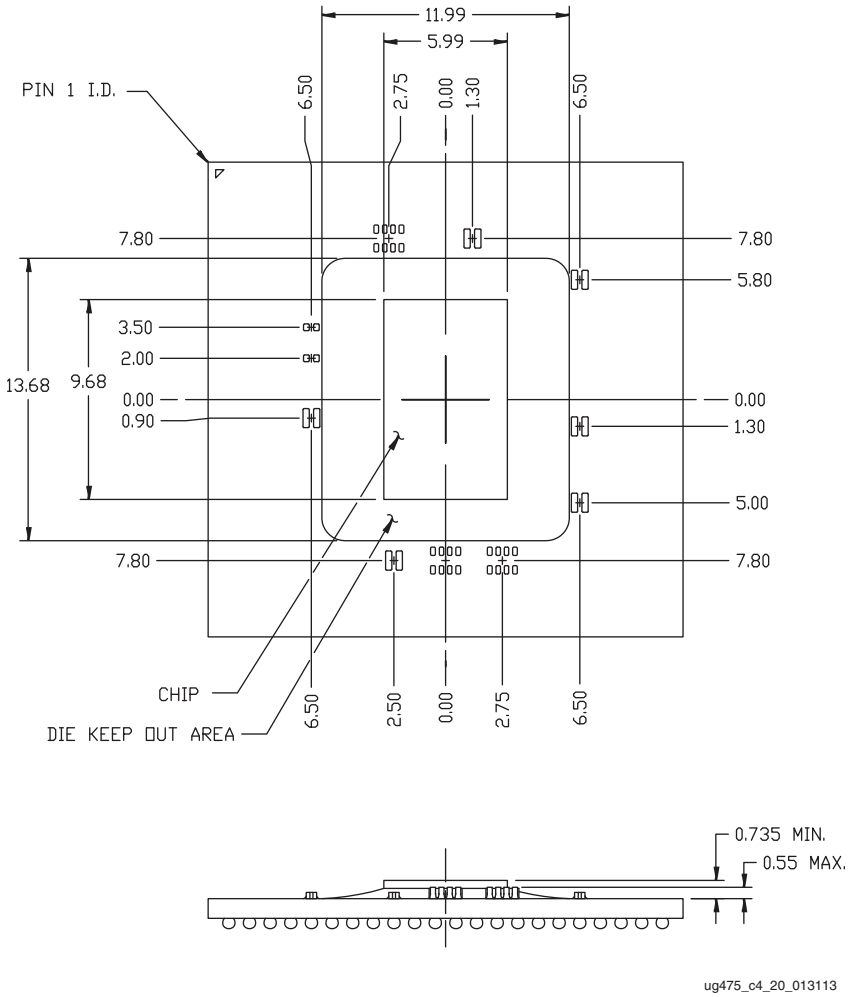


Figure 4-12: **XC7K70T FB/FBG484 Die Dimensions with Capacitor Locations**

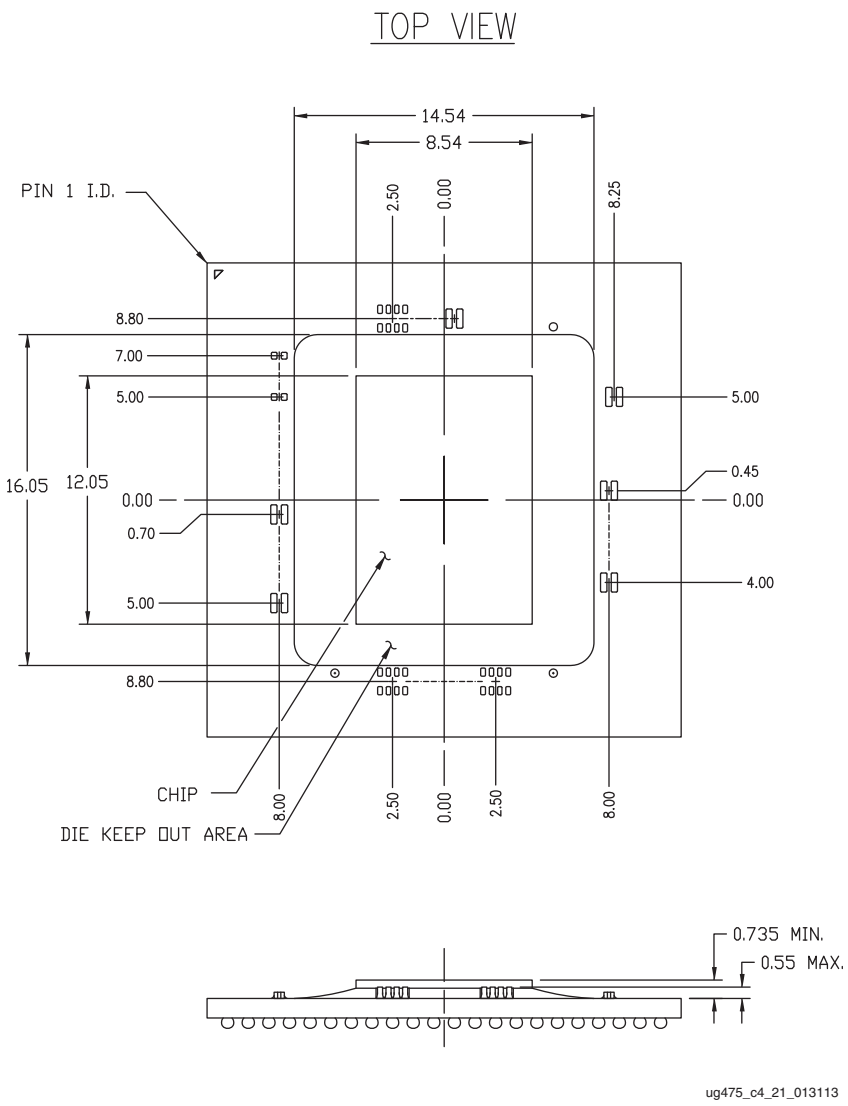
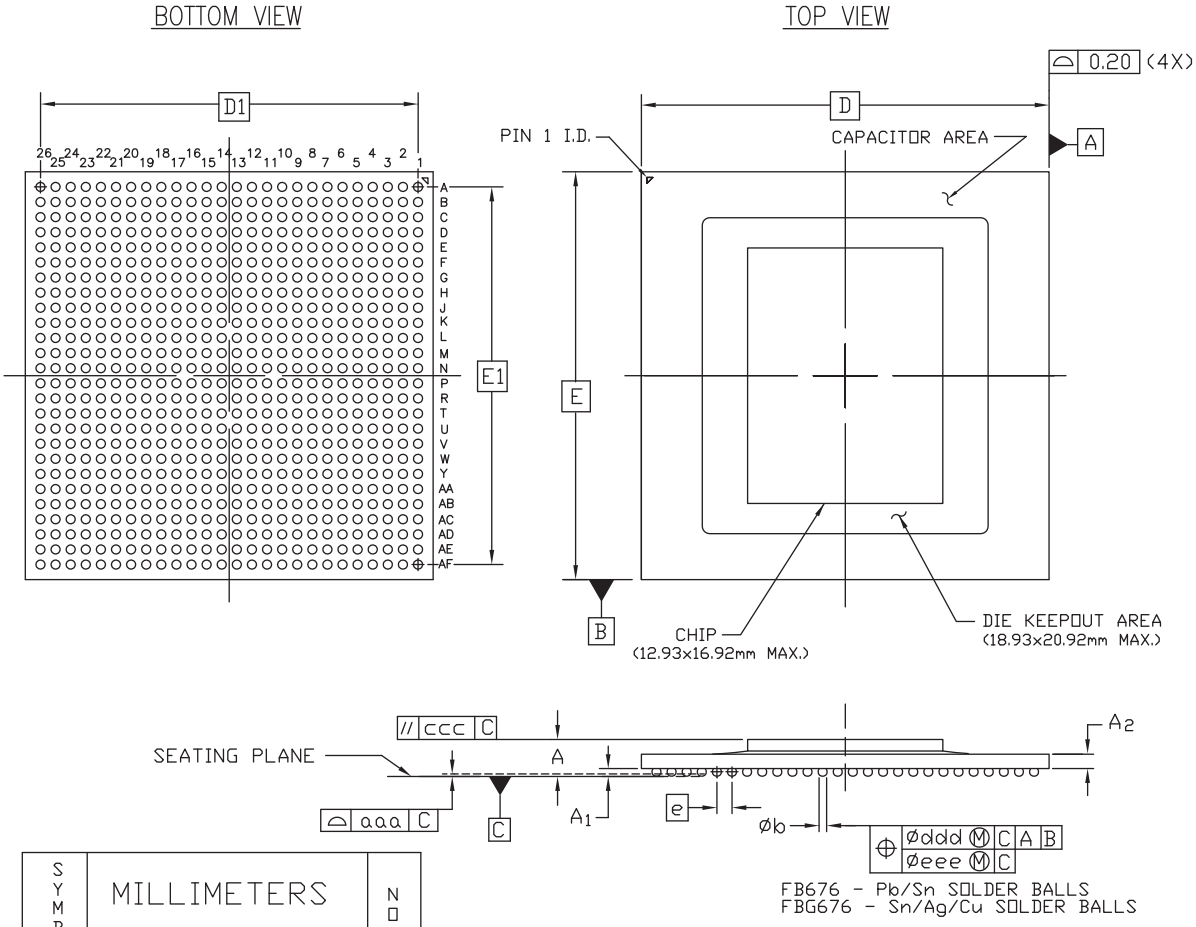


Figure 4-13: **XC7K160T FB/FBG484 Die Dimensions with Capacitor Locations**

FB/FBG676 Flip-Chip Lidless BGA (Kintex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.14	2.34	2.54	
A_1	0.40	0.50	0.60	
A_2	0.88	0.98	1.08	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034
4. SEE FOLLOWING PAGES FOR SPECIFIC DIE SIZE AND CHIP CAPACITOR LOCATION

ug475_c4_02_020713

Figure 4-14: **FB/FBG676 Flip-Chip Lidless BGA Package Specifications for Kintex-7 FPGAs**

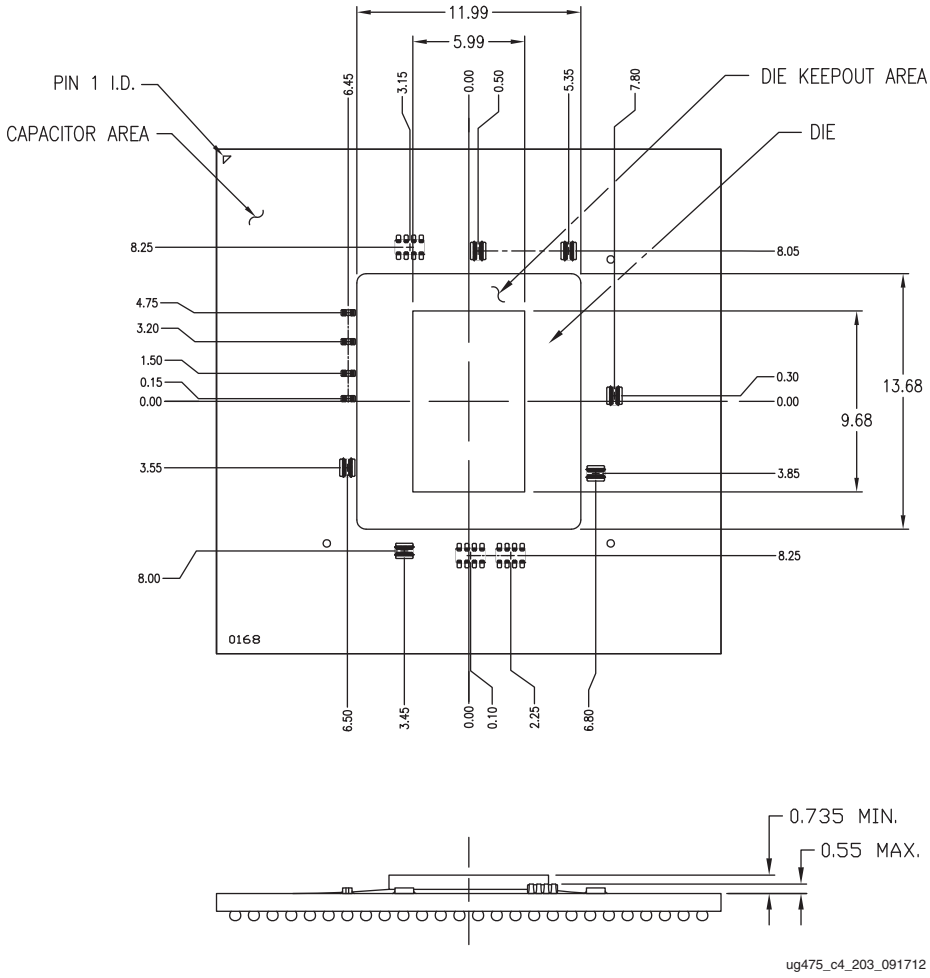


Figure 4-15: **XC7K70T FB/FBG676 Die Dimensions with Capacitor Locations**

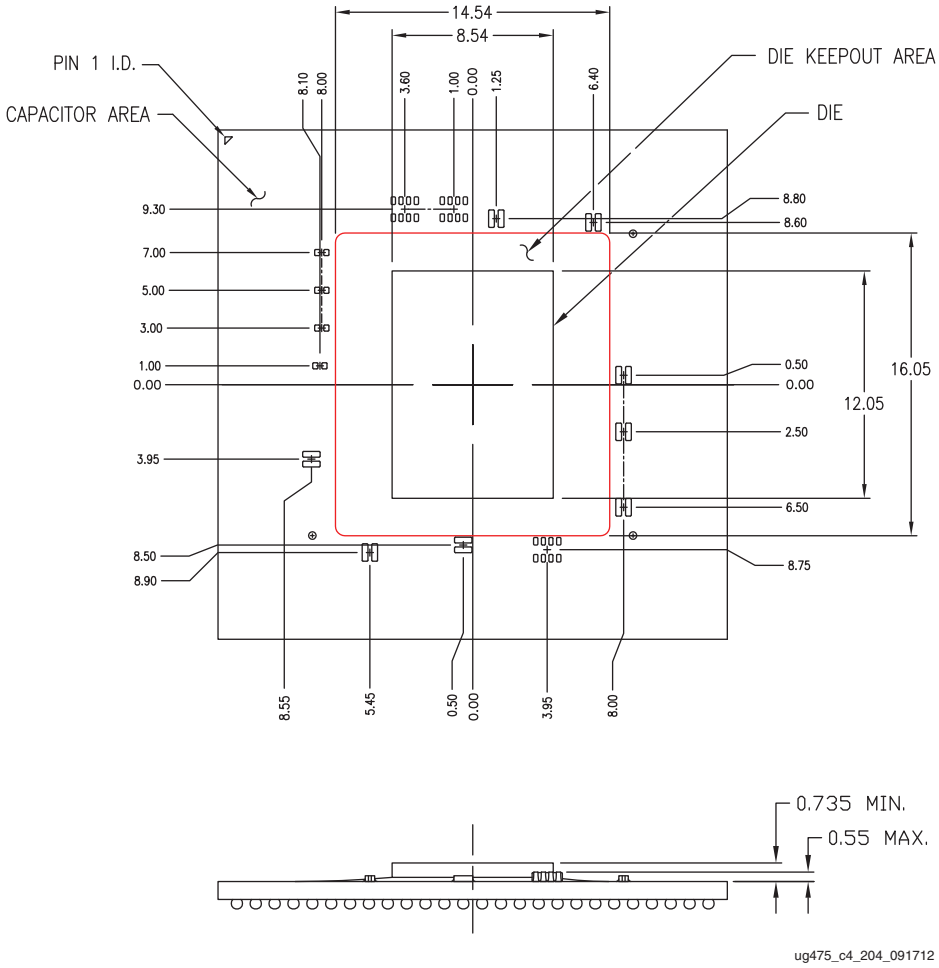


Figure 4-16: **XC7K160T FB/FBG676 Die Dimensions with Capacitor Locations**

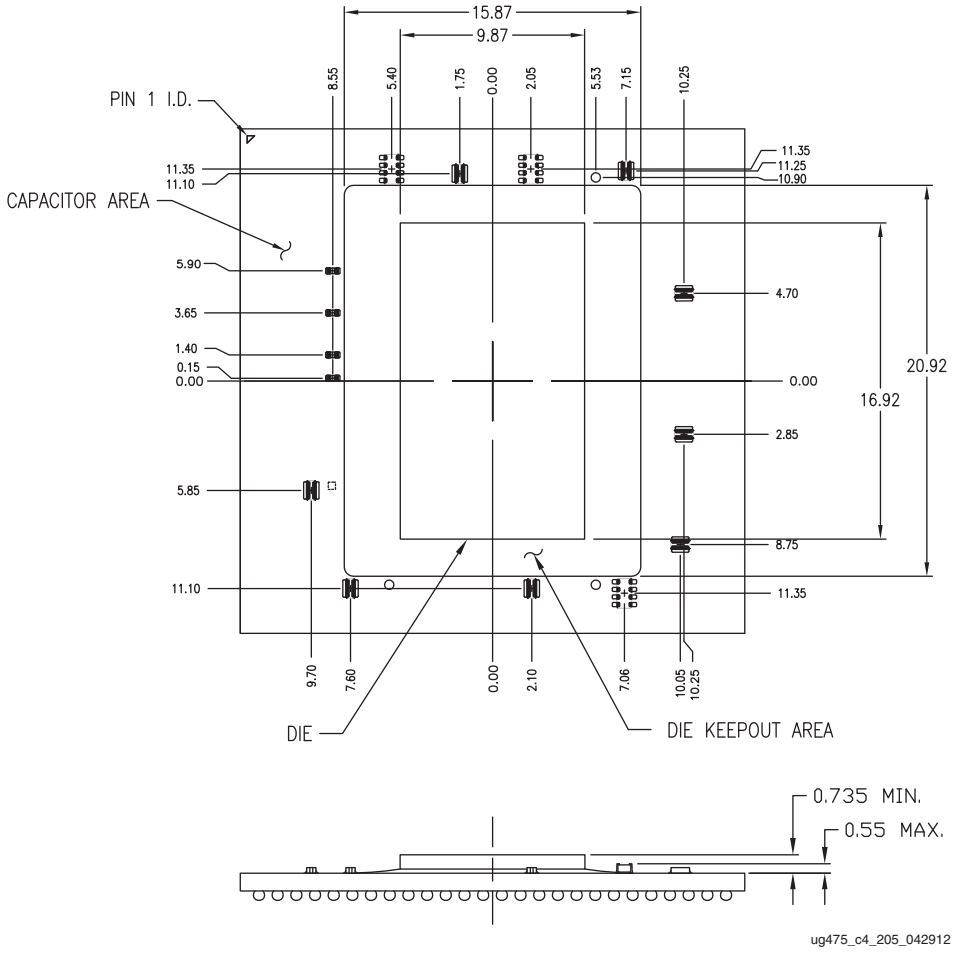


Figure 4-17: **XC7K325T FB/FBG676 Die Dimensions with Capacitor Locations**

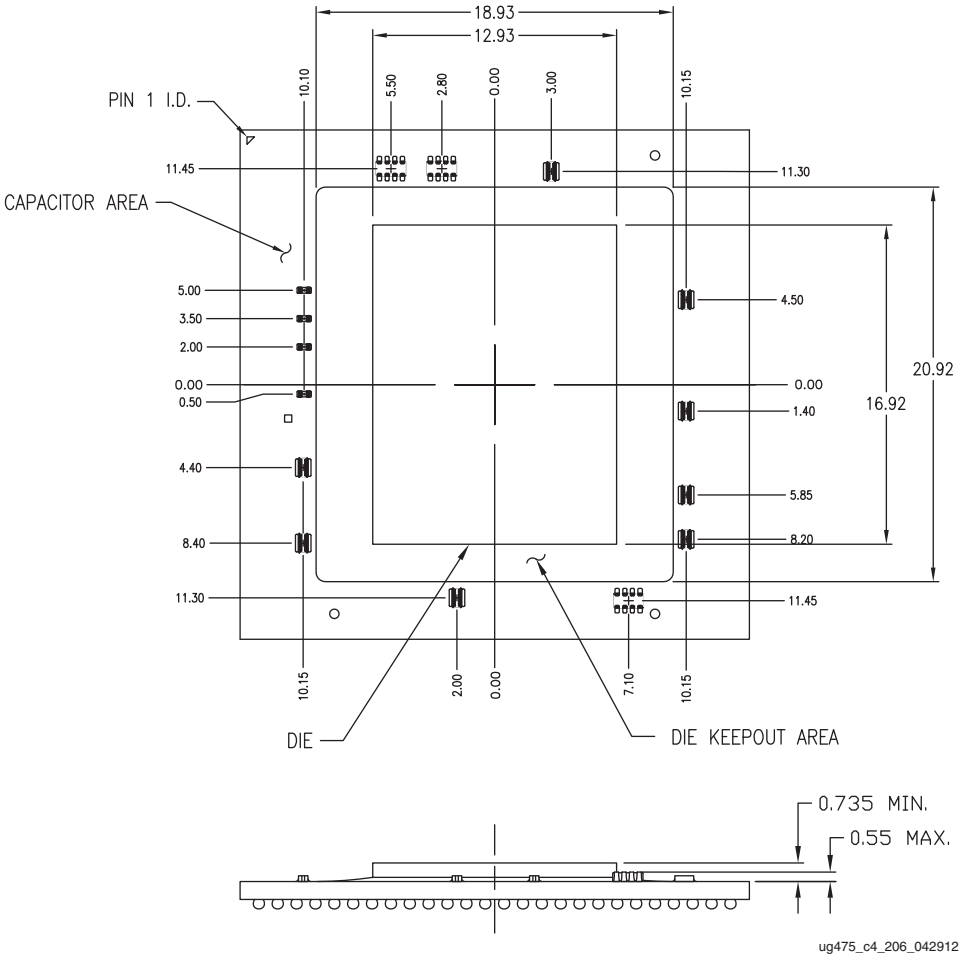
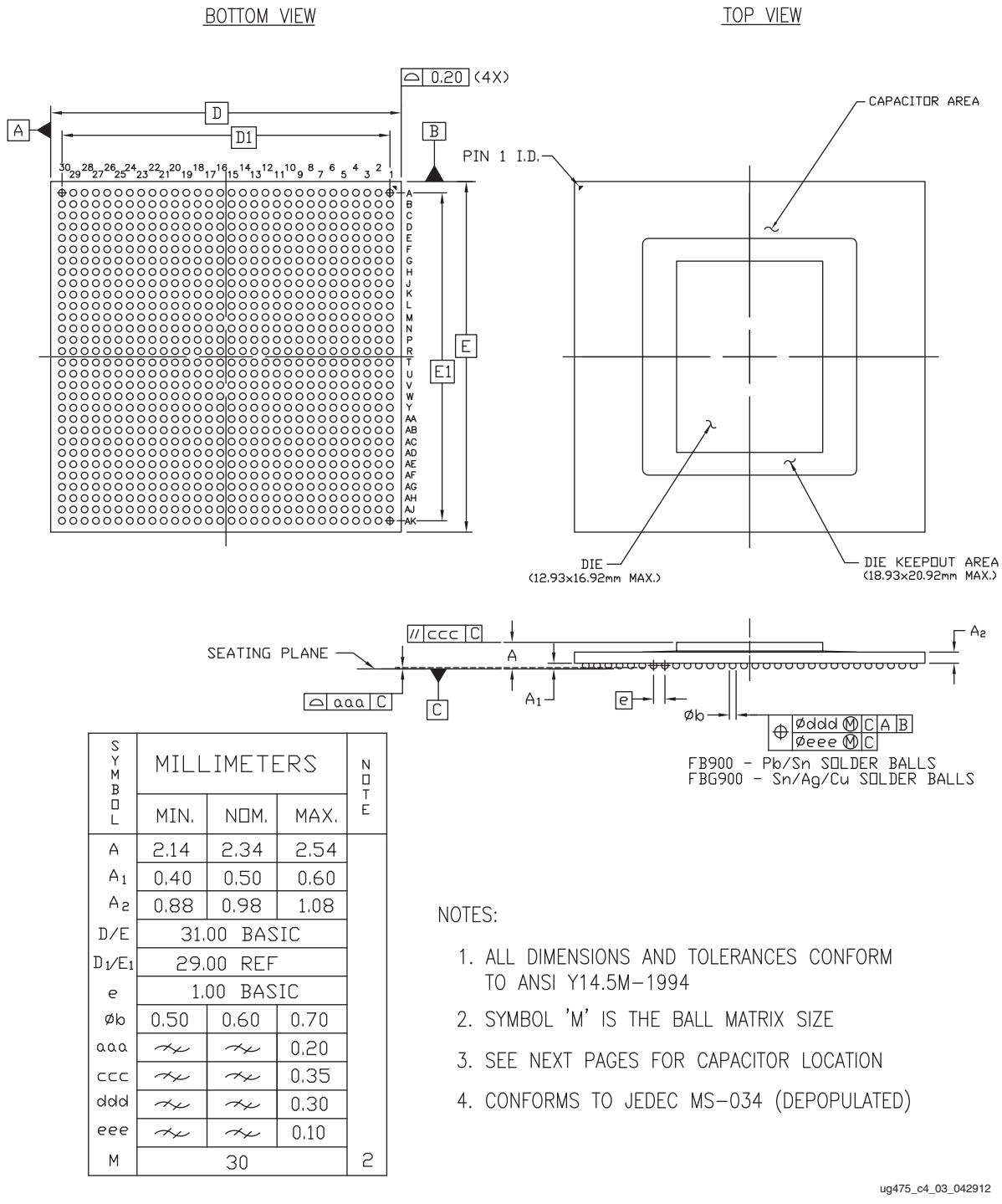


Figure 4-18: **XC7K410T FB/FBG676 Die Dimensions with Capacitor Locations**

FB/FBG900 Flip-Chip Lidless BGA (Kintex-7 FPGAs) (1.0 mm Pitch)



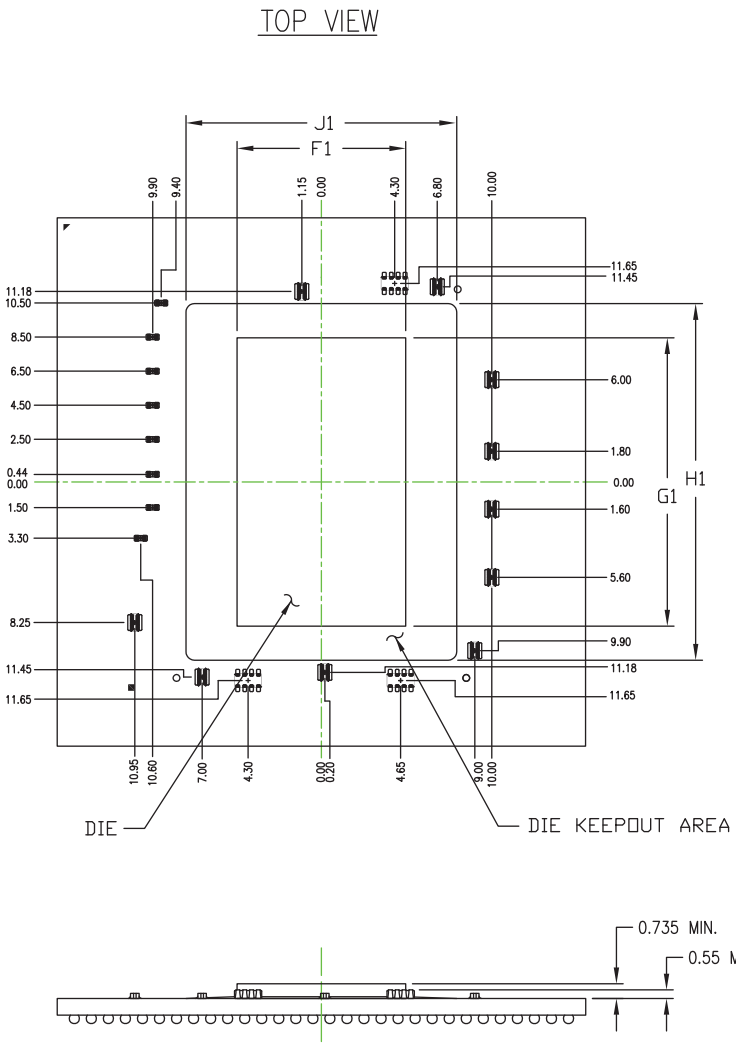
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.14	2.34	2.54	
A_1	0.40	0.50	0.60	
A_2	0.88	0.98	1.08	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	30			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. SEE NEXT PAGES FOR CAPACITOR LOCATION
4. CONFORMS TO JEDEC MS–034 (DEPOPULATED)

ug475_c4_03_042912

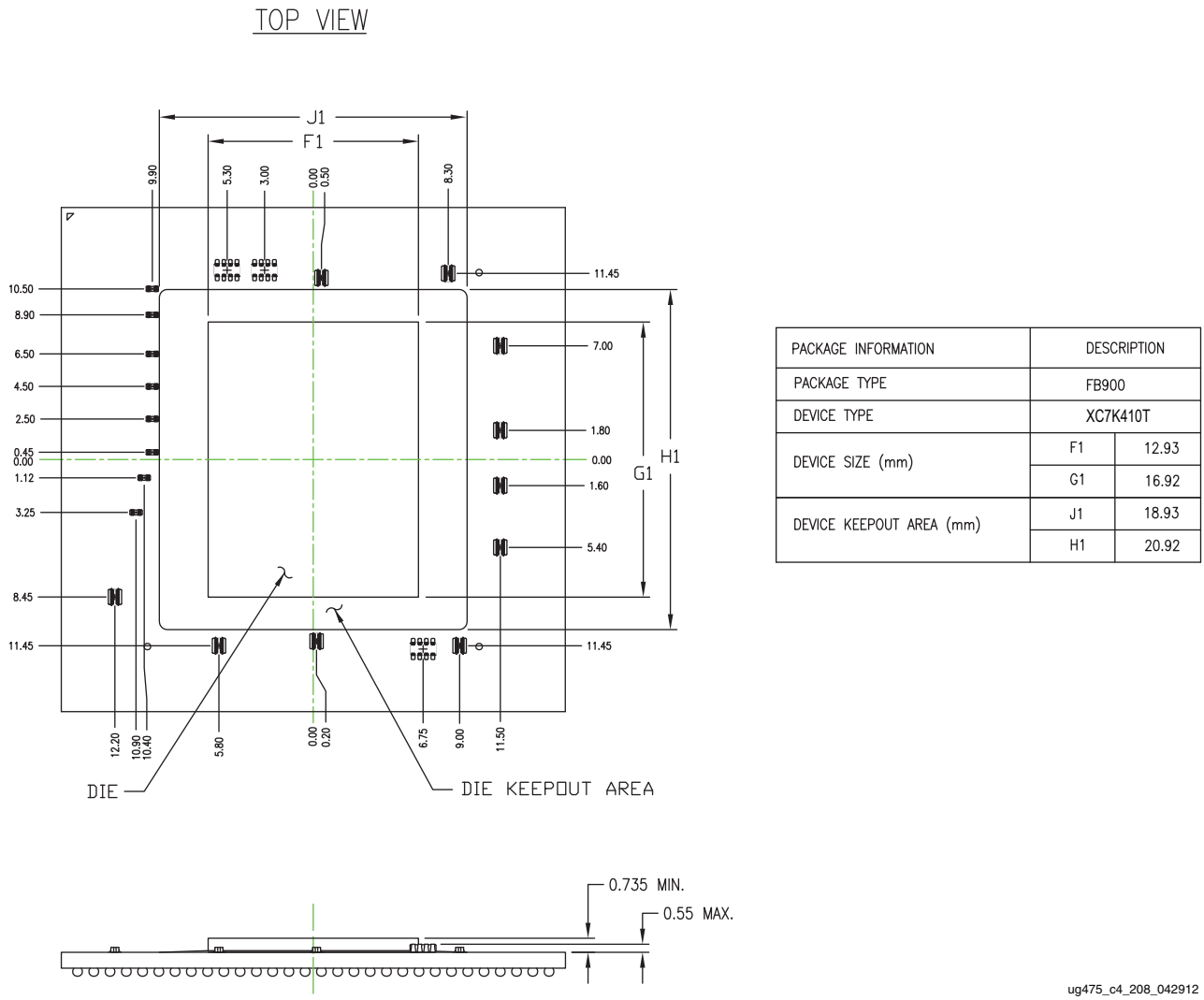
Figure 4-19: **FB/FBG900 Flip-Chip Lidless BGA Package Specifications for Kintex-7 FPGAs**



PACKAGE INFORMATION	DESCRIPTION	
PACKAGE TYPE	FB900	
DEVICE TYPE	XC7K325T	
DEVICE SIZE (mm)	F1	9.89
	G1	16.92
DEVICE KEEPOUT AREA (mm)	J1	15.89
	H1	20.92

ug475_c4_207_042912

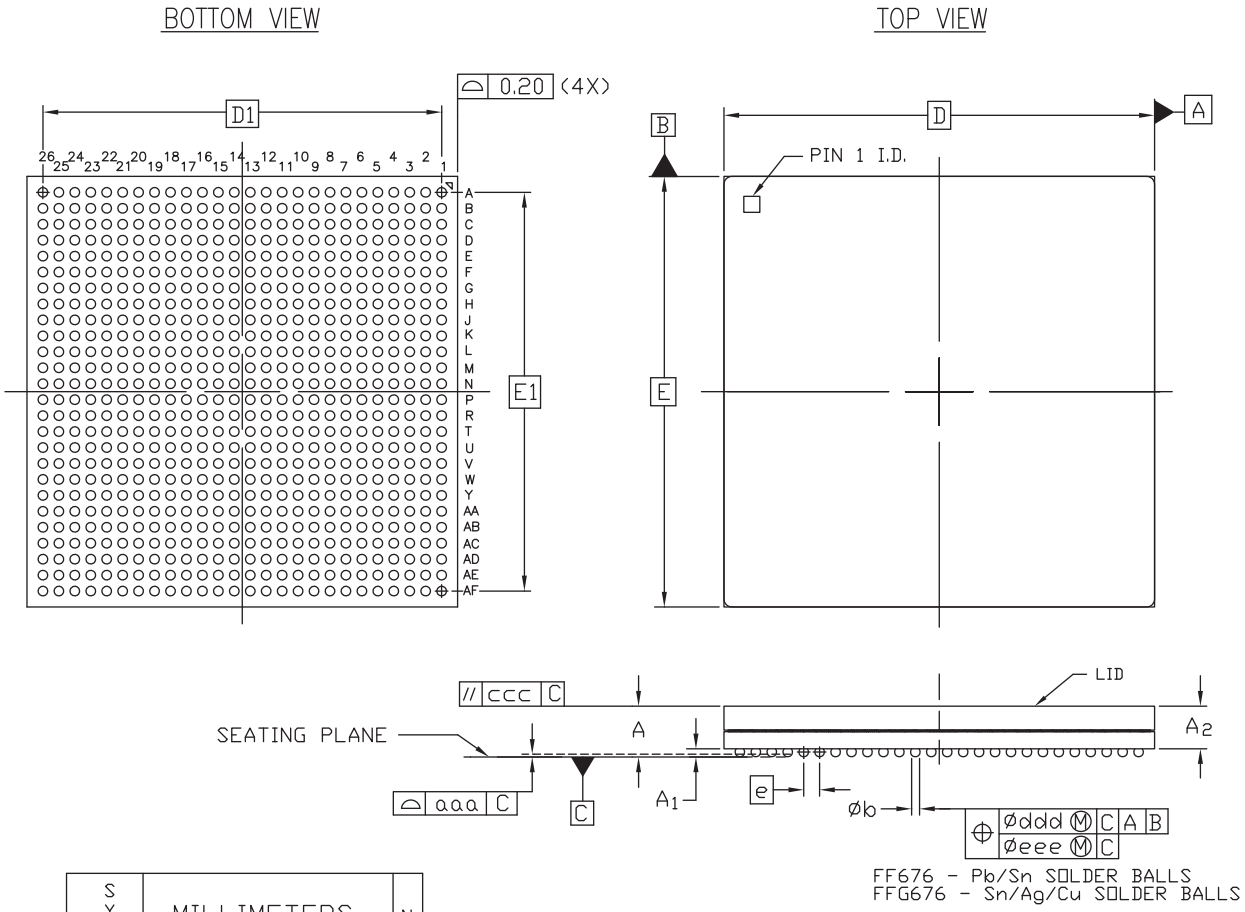
Figure 4-20: **XC7K325T FB/FBG900 Die Dimensions with Capacitor Locations**



PACKAGE INFORMATION	DESCRIPTION	
PACKAGE TYPE	FB900	
DEVICE TYPE	XC7K410T	
DEVICE SIZE (mm)	F1	12.93
	G1	16.92
DEVICE KEEPOUT AREA (mm)	J1	18.93
	H1	20.92

Figure 4-21: **XC7K410T FB/FBG900 Die Dimensions with Capacitor Locations**

FF/FFG676 Flip-Chip BGA (Kintex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.97	3.17	3.37	
A_1	0.40	0.50	0.60	
A_2	2.57	~	2.77	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	26			2

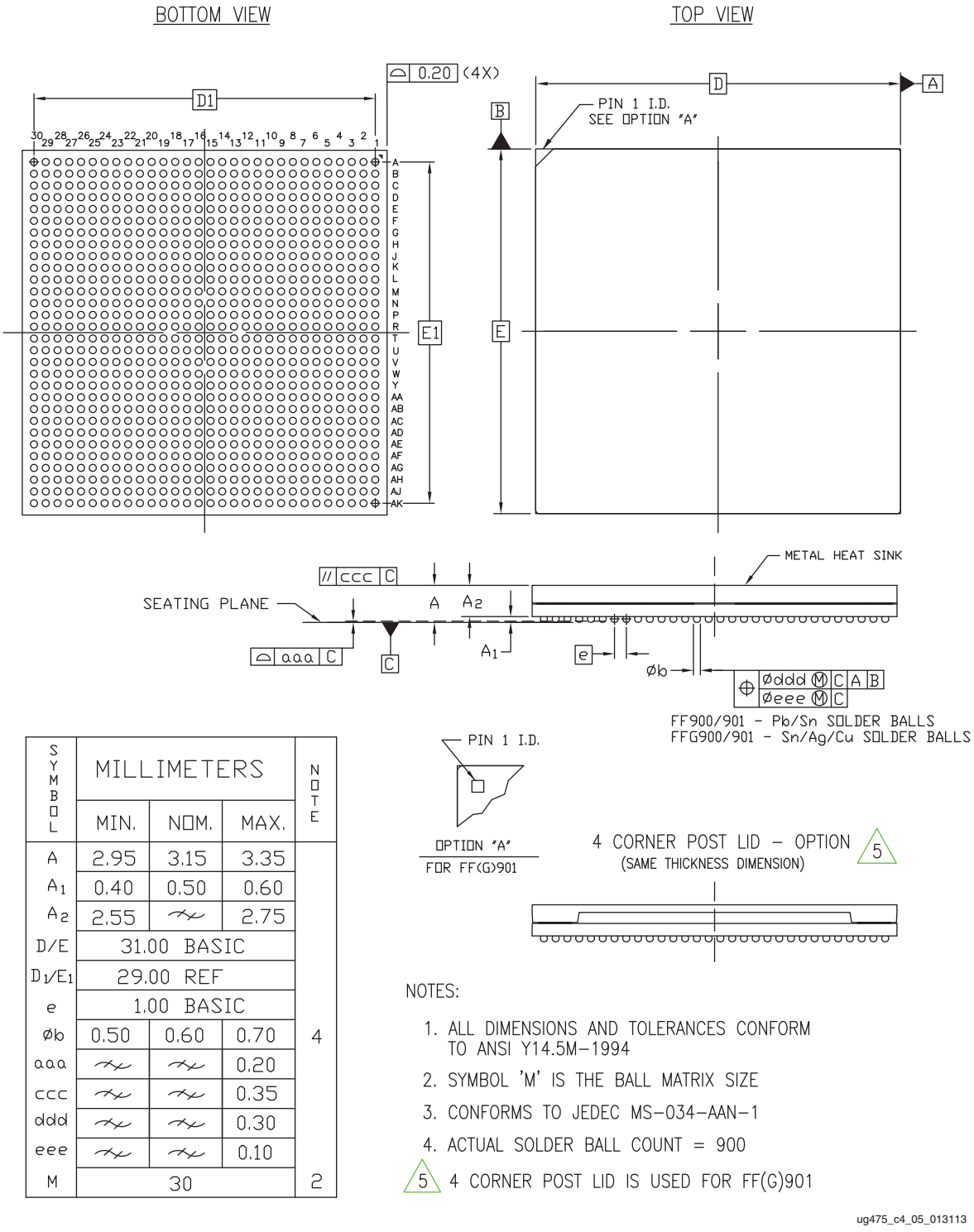
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1

ug475_c4_04_050312

Figure 4-22: **FF/FFG676 Flip-Chip BGA Package Specifications for Kintex-7 FPGAs**

FF/FFG900 and FF/FFG901 Flip-Chip BGA (Kintex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.95	3.15	3.35	
A_1	0.40	0.50	0.60	
A_2	2.55	~	2.75	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	4
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	30			2

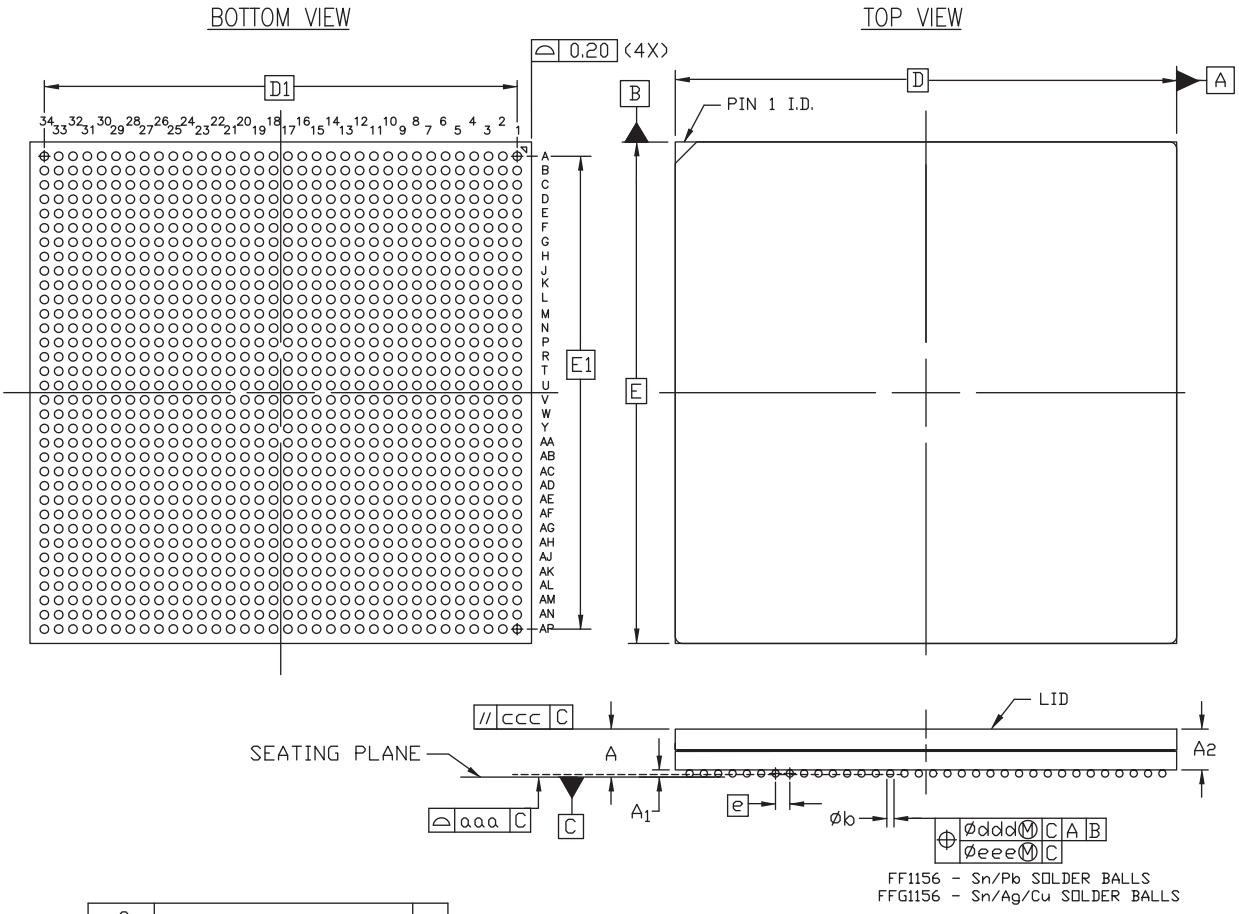
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS-034-AAN-1
4. ACTUAL SOLDER BALL COUNT = 900
5. 4 CORNER POST LID IS USED FOR FF(G)901

ug475_c4_05_013113

Figure 4-23: **FF/FFG900 and FF/FFG901 Flip-Chip BGA Package Specifications for Kintex-7 FPGAs**

FF/FFG1156 Flip-Chip BGA (Kintex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.95	~~	3.35	
A_1	0.40	0.50	0.60	
A_2	2.55	~~	2.75	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	4
aaa	~~	~~	0.20	
ccc	~~	~~	0.35	
ddd	~~	~~	0.30	
eee	~~	~~	0.10	
M	34			2

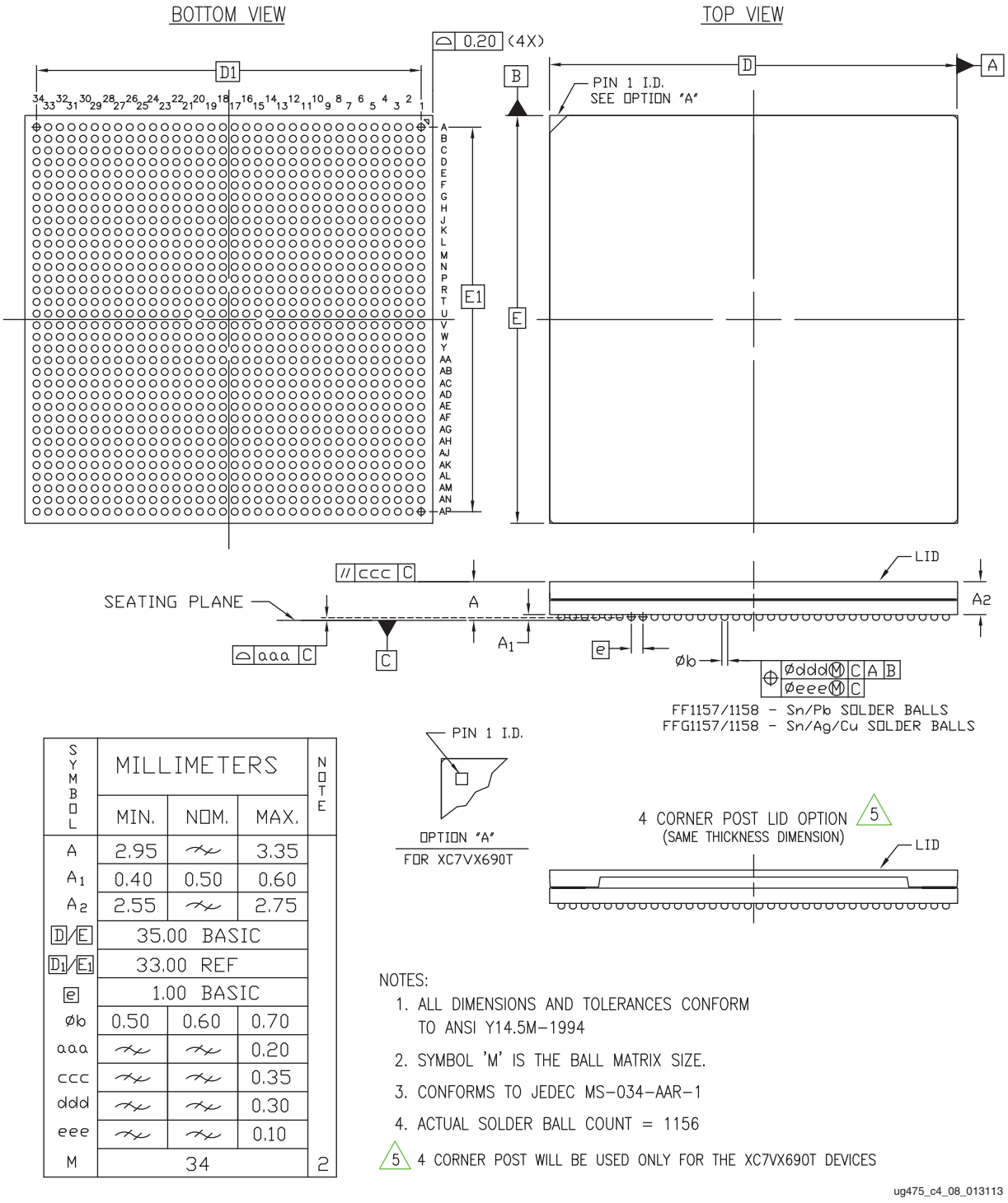
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAR–1
4. ACTUAL SOLDER BALL COUNT = 1156
5. THIS PACKAGE IS USED FOR KINTEX®–7 FPGAs REFER TO PK384 FOR THE MECHANICAL DRAWING OF THE FF1156 PACKAGE USED FOR VIRTEX®–5 FPGAS AND PK401 FOR VIRTEX®–6 FPGAS

ug475_c4_07_051512

Figure 4-24: **FF/FFG1156 Flip-Chip BGA Package Specification for Kintex-7 FPGAs**

FF/FFG1157 and FF/FFG1158 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.95	~~	3.35	
A_1	0.40	0.50	0.60	
A_2	2.55	~~	2.75	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~~	~~	0.20	
ccc	~~	~~	0.35	
ddd	~~	~~	0.30	
eee	~~	~~	0.10	
M	34			2

NOTES:

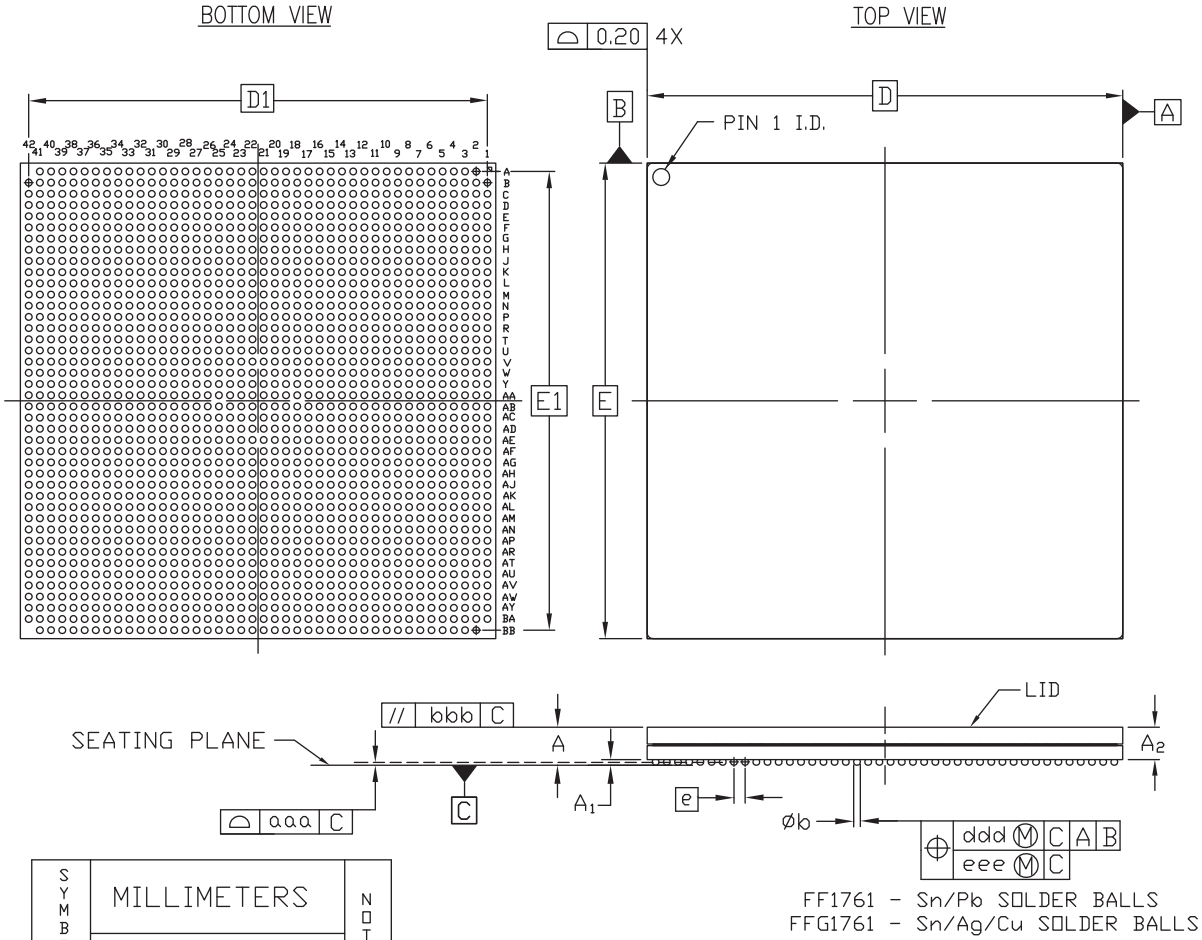
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1
4. ACTUAL SOLDER BALL COUNT = 1156

5 4 CORNER POST WILL BE USED ONLY FOR THE XC7VX690T DEVICES

ug475_c4_08_013113

Figure 4-25: **FF/FFG1157 and FF/FFG1158 Flip-Chip BGA Package Specification for Virtex-7 FPGAs**

FF/FFG1761 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.10		3.50	
A_1	0.40	0.50	0.60	
A_2	2.70		2.90	
D/E	42.50 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	42			2

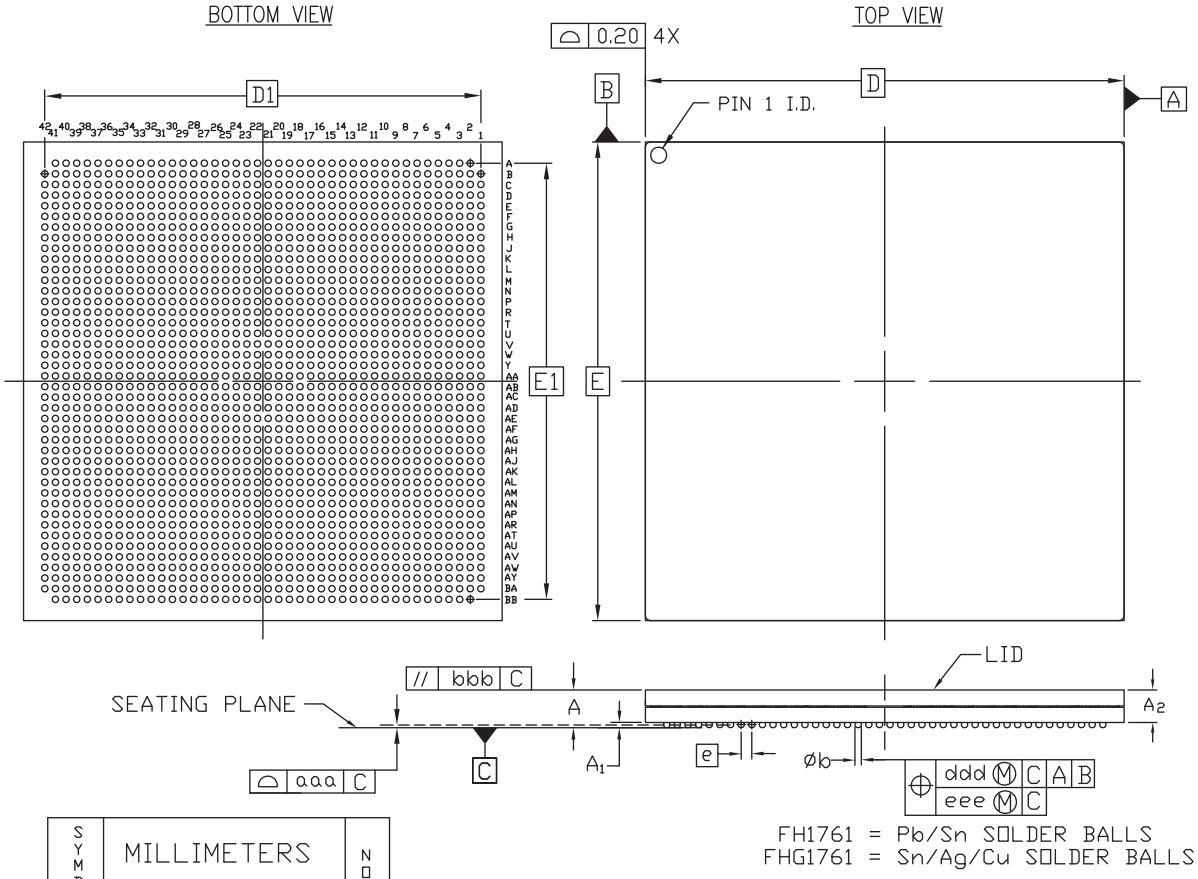
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)
4. ACTUAL SOLDER BALL COUNT = 1760

ug475_c4_09_091411

Figure 4-26: **FF/FFG1761 Flip-Chip BGA Package Specification for Virtex-7 FPGAs**

FH/FHG1761 Flip-Chip BGA (Virtex-7 T FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.25		3.75	
A_1	0.40	0.50	0.60	
A_2	2.85		3.15	
D/E	45.00 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.30	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	42			2

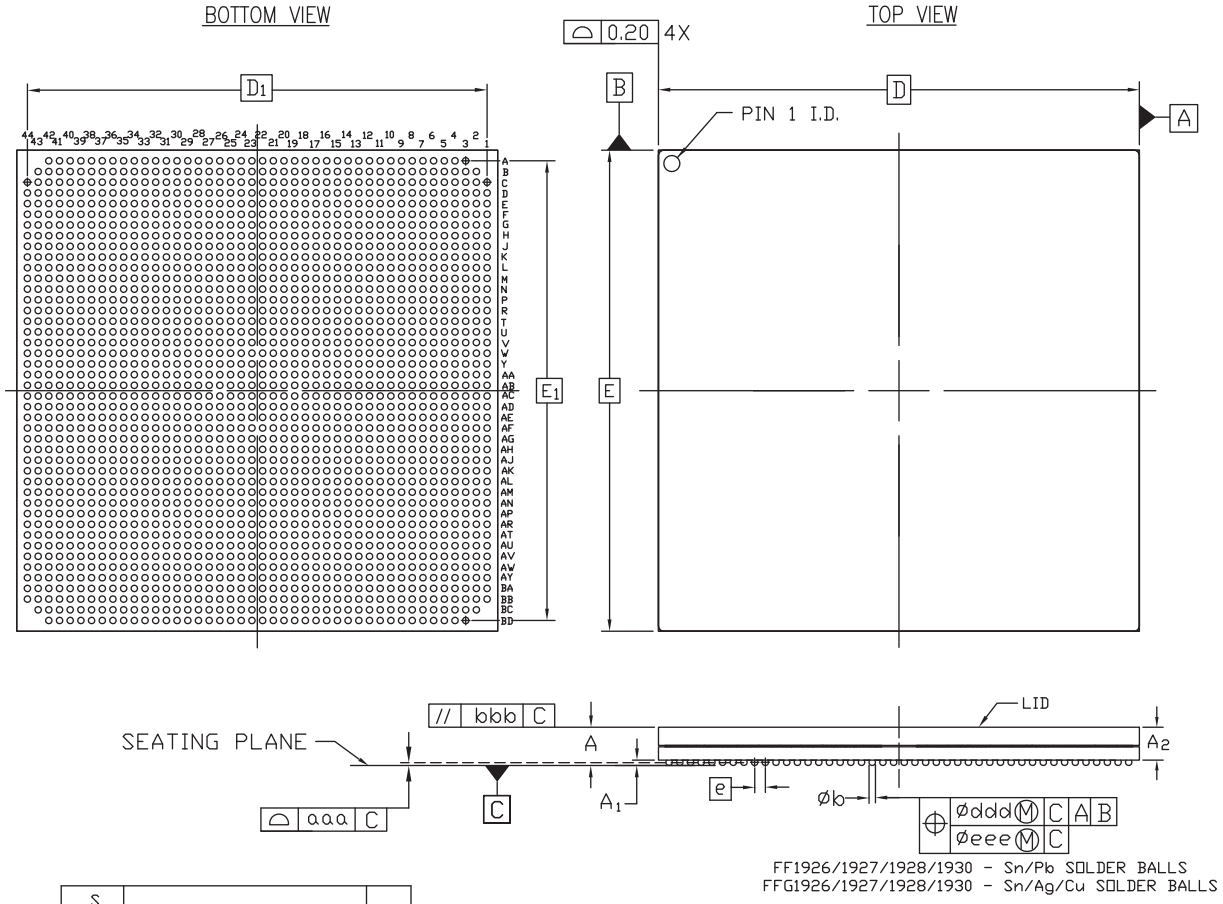
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)
4. ACTUAL SOLDER BALL COUNT = 1760

ug475_c4_10_092412

Figure 4-27: **FH/FHG1761 Flip-Chip BGA Package Specification for Virtex-7 T FPGAs**

FF/FFG1926, FF/FFG1927, FF/FFG1928, and FF/FFG1930 Flip-Chip BGA (Virtex-7 XT FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.25		3.65	
A_1	0.40	0.50	0.60	
A_2	2.85		3.05	
D/E	45.00 BASIC			
D_1/E_1	43.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	3
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	44			2

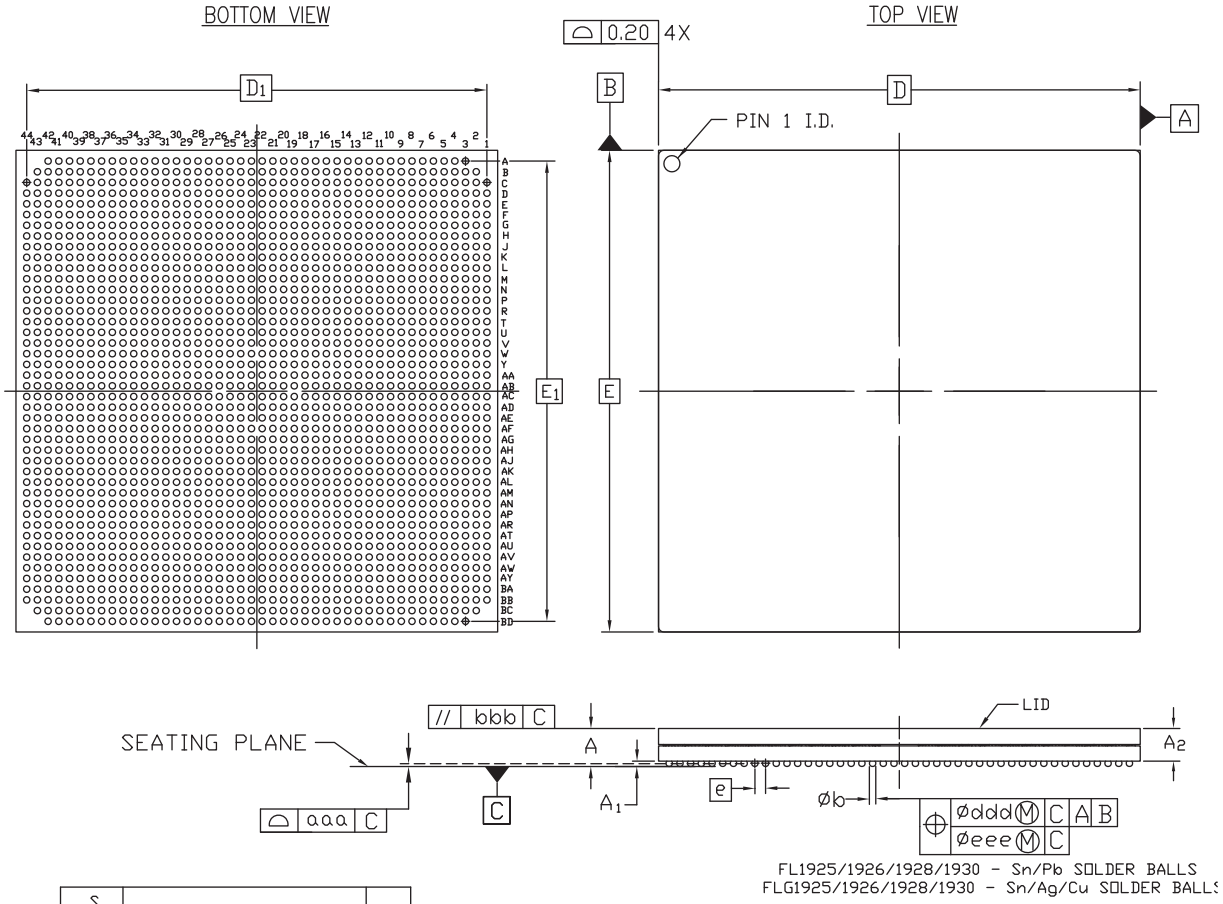
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. ACTUAL SOLDER BALL COUNT = 1924
4. CONFORMS TO JEDEC MS–034–AAW–1 (DEPOPULATED)

ug475_c4_11_091712

Figure 4-28: **FF/FFG1926, FF/FFG1927, FF/FFG1928, and FF/FFG1930 Flip-Chip BGA Package Specification for Virtex-7 XT FPGAs**

FL/FLG1925, FL/FLG1926, FL/FLG1928, and FL/FLG1930 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.25		3.75	
A_1	0.40	0.50	0.60	
A_2	2.85		3.15	
D/E	45.00 BASIC			
D_1/E_1	43.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	3
aaa			0.30	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	44			2

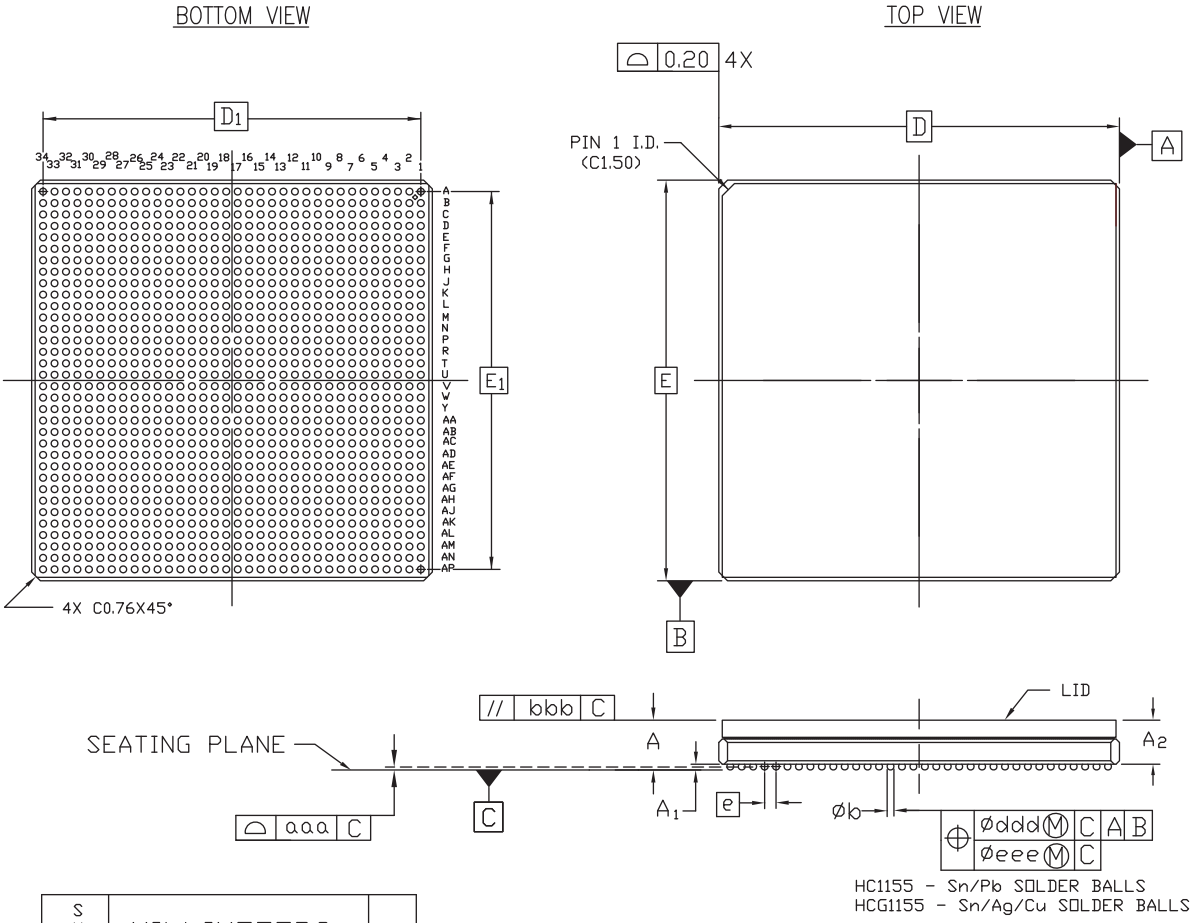
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. ACTUAL SOLDER BALL COUNT = 1924

ug475_c4_12_091712

Figure 4-29: **FL/FLG1925, FL/FLG1926, FL/FLG1928, and FL/FLG1930 Flip-Chip BGA Package Specification for Virtex-7 FPGAs**

HCG1155 Ceramic Flip-Chip BGA (Virtex-7 HT FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	4.20		5.00	
A_1	0.40	0.50	0.60	
A_2	3.80		4.40	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	3
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	44			2

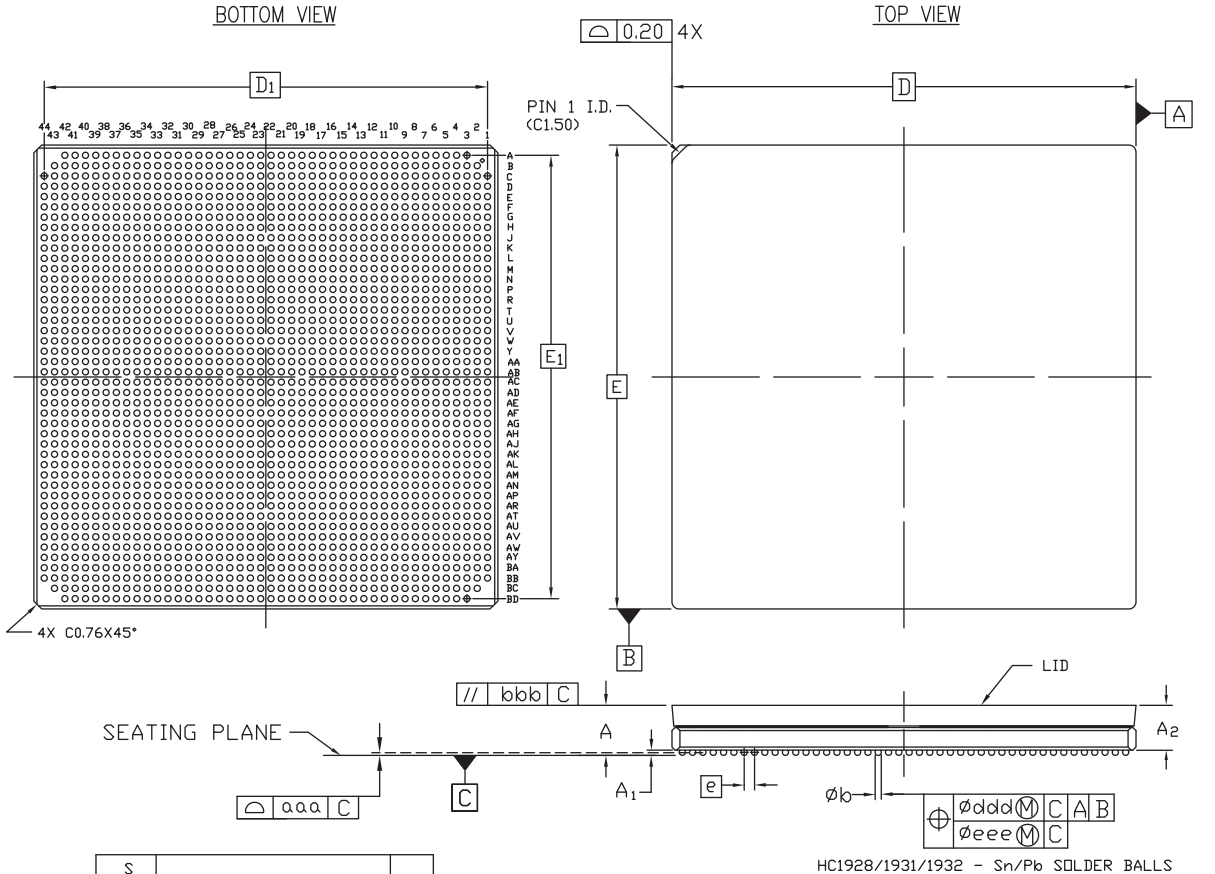
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE
3. ACTUAL SOLDER BALL COUNT = 1156

ug475_c4_18_070212

Figure 4-30: **HCG1155 Ceramic Flip-Chip BGA Package Specification for Virtex-7 HT FPGAs**

HCG1931 and HCG1932 Ceramic Flip-Chip BGA (Virtex-7 HT FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	4.50		5.30	
A_1	0.40	0.50	0.60	
A_2	4.10		4.70	
D/E	45.00 BASIC			
D_1/E_1	43.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	3
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	44			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. ACTUAL SOLDER BALL COUNT = 1924

ug475_c4_19_070212

Figure 4-31: **HCG1931 and HCG1932 Ceramic Flip-Chip BGA Package Specification for Virtex-7 HT FPGAs**

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Chapter 5

Thermal Specifications

Summary

This chapter provides thermal data associated with 7 series FPGAs packages. The following topics are discussed:

- Introduction
- Thermal Management Strategy
- Some Thermal Management Options
- Support for Compact Thermal Models (CTM)
- Soldering Guidelines
- References

Introduction

7 series FPGAs are offered exclusively in thermally efficient flip-chip BGA packages. These 0.8 mm and 1.0 mm flip-chip packages range in pin-count from the smaller 15 x 15 mm CSG324 to the 45 x 45 mm FFG1930 and HCG1932. This suite of packages is used to address the various power requirements of the 7 series devices. All 7 series devices are implemented in the 28 nm process technology.

Similar to Virtex®-6 FPGAs, all 7 series devices feature the versatile SelectIO™ resources that support a variety of I/O standards. They also include analog-to-digital converters (XADC), DSPs, and other traditional features and blocks (such as block RAM) contained in earlier Virtex products.

In line with Moore's law, the transistor count in this family of devices has been increased substantially. Though several innovative features at the silicon level have been deployed to minimize power dissipation, including leakage at the 28 nm node, these products have more densely packed transistors and embedded blocks with the capability to run faster than before. Thus, a fully configured 7 series FPGA design that exploits the fabric speed and incorporates several embedded circuits and systems can present power consumption challenges that must be managed.

Unlike features in an ASIC or a microprocessor, the combination of FPGA features used in a user application are not known to the component supplier. Therefore, it remains a challenge for Xilinx to predict the power requirements of a given FPGA when it leaves the factory. Accurate estimates are obtained when the board design takes shape. For this purpose, Xilinx offers and supports a suite of integrated device power analysis tools to help users quickly and accurately estimate their design power requirements. 7 series devices are supported similarly to previous FPGA products. The uncertainty of design power requirements makes it difficult to apply canned thermal solutions to fit all users.

Therefore, Xilinx devices do not come with preset thermal solutions. The user's operating conditions dictate the appropriate solution.

Table 5-1 shows the thermal resistance data for 7 series devices (grouped in the packages offered). The data includes junction-to-ambient in still air, junction-to-case, and junction-to-board data based on standard JEDEC four-layer measurements.

- Thermal data is available on the Xilinx website at:

  http://www.xilinx.com/cgi-bin/thermal/thermal.pl.
- Compact package thermal models for these products are available on the Xilinx support download center (under the Device Model tab) at:

  http://www.xilinx.com/support/download/index.htm

Table 5-1: **Thermal Resistance Data—All Devices**

Package	Package Body Size	Devices	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W) @ 250 LFM	θ_{JA} (°C/W) @ 500 LFM	θ_{JA} (°C/W) @ 750 LFM
Artix-7 FPGAs								
CS/CSG324	15 x 15	XC7A100T	18.3	5.8	3.23	14.1	13.0	12.3
FT/FTG256	17 x 17	XC7A100T	18.2	6.9	3.33	14.1	12.9	12.2
SBG484	19 x 19	XC7A200T	14.8	4.9	0.06	10.9	9.8	9.2
FB/FBG484	23 x 23	XC7A200T	13.9	4.8	0.06	9.9	8.8	8.3
FG/FGG484	23 x 23	XC7A100T	16.1	6.8	3.82	12.1	11.0	10.4
FB/FBG676	27 x 27	XC7A200T	13.0	4.6	0.07	9.2	8.2	7.7
FG/FGG676	27 x 27	XC7A100T	15.3	6.7	3.67	11.2	10.2	9.7
FF/FFG1156	35 x 35	XC7A200T	9.1	2.6	0.30	6.1	5.2	4.7
Kintex-7 FPGAs								
FB/FBG484	23 x 23	XC7K70T	15.9	6.5	0.16	11.7	10.6	10.0
		XC7K160T	13.6	5.0	0.07	10.5	9.4	8.9
FB/FBG676	27 x 27	XC7K70T	15.8	6.5	0.16	11.7	10.8	10.2
		XC7K160T	14.0	5.0	0.07	9.7	8.8	8.3
		XC7K325T	13.1	4.1	0.04	9.1	8.1	7.5
		XC7K410T	11.9	3.5	0.03	8.6	7.6	7.1
FF/FFG676	27 x 27	XC7K160T	11.8	4.0	0.38	7.5	6.4	5.8
		XC7K325T	10.0	3.6	0.23	7.3	6.2	5.6
		XC7K410T	9.7	3.3	0.17	7.0	6.0	5.5
FB/FBG900	31 x 31	XC7K325T	11.9	4.1	0.04	8.9	7.9	7.3
		XC7K410T	10.7	3.6	0.03	8.3	7.3	6.7
FF/FFG900	31 x 31	XC7K325T	8.6	2.6	0.24	6.3	5.4	5.0
		XC7K410T	8.2	2.4	0.19	6.0	5.2	4.8

Table 5-1: **Thermal Resistance Data—All Devices *(Cont'd)***

Package	Package Body Size	Devices	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W) @ 250 LFM	θ_{JA} (°C/W) @ 500 LFM	θ_{JA} (°C/W) @ 750 LFM
FF/FFG901	31 x 31	XC7K355T	8.2	3.2	0.20	6.2	5.2	4.6
		XC7K420T	8.1	3.2	0.19	6.0	5.2	4.7
		XC7K480T	7.6	2.9	0.15	5.8	5.1	4.6
FF/FFG1156	35 x 35	XC7K420T	7.3	3.2	0.19	5.8	4.9	4.4
		XC7K480T	6.8	2.2	0.16	5.4	4.6	4.2
Virtex-7 T FPGAs								
FF/FFG1157	35 x 35	XC7V585T	8.7	2.3	0.05	5.6	4.7	4.3
FF/FFG1761	42.5 x 42.5	XC7V585T	7.6	2.2	0.05	4.9	4.1	3.7
FH/FHG1761	42.5 x 42.5	XC7V2000T	7.0	3.3	0.04	4.3	3.5	3.1
FL/FLG1925	45 x 45	XC7V2000T	6.9	1.6	0.04	4.3	3.5	3.1
Virtex-7 XT FPGAs								
FF/FFG1157	35 x 35	XC7VX330T	7.4	2.3	0.18	5.6	4.8	4.4
		XC7VX415T	7.0	2.1	0.14	5.4	4.7	4.3
		XC7VX485T	9.0	2.1	0.13	5.6	4.8	4.3
		XC7VX690T	6.1	2.0	0.04	4.8	4.2	3.8
FF/FFG1158	35 x 35	XC7VX415T	6.8	2.2	0.13	5.4	4.7	4.3
		XC7VX485T	9.0	2.1	0.13	5.6	4.8	4.3
		XC7VX550T	6.5	2.1	0.09	5.2	4.5	4.2
		XC7VX690T	6.2	1.9	0.03	4.8	4.1	3.8
FF/FFG1761	42.5 x 42.5	XC7VX330T	6.4	2.3	0.19	4.8	4.1	3.7
		XC7VX485T	7.8	1.9	0.11	4.9	4.1	3.7
		XC7VX690T	5.6	1.8	0.08	4.5	3.8	3.5
FF/FFG1926	45 x 45	XC7VX690T	5.1	1.8	0.08	4.1	3.5	3.2
		XC7VX980T	4.8	1.7	0.04	3.8	3.2	2.9
FF/FFG1927	45 x 45	XC7VX415T	5.6	1.8	0.14	4.3	3.7	3.3
		XC7VX485T	7.4	1.9	0.11	4.8	3.9	3.5
		XC7VX550T	5.4	1.8	0.09	4.2	3.6	3.3
		XC7VX690T	4.9	1.7	0.07	4.1	3.5	3.2
FF/FFG1928	45 x 45	XC7VX980T	4.8	1.7	0.04	4.0	3.4	3.1
FF/FFG1930	45 x 45	XC7VX485T	7.4	1.9	0.10	4.8	3.9	3.5
		XC7VX690T	5.4	1.8	0.08	4.0	3.4	3.0
		XC7VX980T	5.0	1.7	0.04	3.8	3.2	2.9

Table 5-1: **Thermal Resistance Data—All Devices *(Cont'd)***

Package	Package Body Size	Devices	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W) @ 250 LFM	θ_{JA} (°C/W) @ 500 LFM	θ_{JA} (°C/W) @ 750 LFM
FL/FLG1926	45 x 45	XC7VX1140T	6.9	1.6	0.04	4.3	3.5	3.1
FL/FLG1928	45 x 45	XC7VX1140T	6.9	1.6	0.04	4.3	3.5	3.1
FL/FLG1930	45 x 45	XC7VX1140T	6.9	1.6	0.04	4.2	3.5	3.1
Virtex-7 HT FPGAs(1)								
HCG1155	35 x 35	XC7VH580T	6.2	1.8	0.09	4.9	4.2	3.7
HCG1931	45 x 45	XC7VH580T	5.1	0.7	0.04	4.0	3.3	3.0
		XC7VH870T						
HCG1932	45 x 45	XC7VH580T	5.2	0.7	0.04	4.0	3.4	3.0
		XC7VH870T						

Notes:

1. The ceramic packages lid composition is AlSiC (Aluminum Silicon Carbide). See the specific package outline in Chapter 5, Thermal Specifications.

Thermal Management Strategy

As described in this section, Xilinx relies on a multi-pronged approach with regards to the heat-dissipating potential of 7 series devices.

Design and Silicon

Power consumption reduction when using 28 nm node 7 series devices is achieved through innovative process and circuit design. For example, transistor static leakage current is minimized by more than 50% by deploying the multi-gate oxide transistors in the power-efficient 7 series architecture.

Despite these improvements and a low operating voltage, the base transistor counts are still large; 7 series devices pack high gate densities. Still, when comparing previous silicon generations, a 7 series FPGA programmable logic implementation has lower power consumption.

However, the increased resources and functionality associated with higher gate density devices and faster switching programmable logic resources implies increased computation with less delay. Also associated with this improved functionality is the potential for better power dissipation due to the silicon and device-based innovations.

Cavity-Up Plastic BGA Packages

BGA is a plastic package technology that utilizes area array solder balls at the bottom of the package to make electrical contact with the circuit board in the users system. The area array format of solder balls reduces package size considerably when compared to leaded products. It also results in improved electrical performance as well as having higher manufacturing yields. The substrate is made of a multi-layer BT (bismaleimide triazene) epoxy-based material. Power and GND pins are grouped together and signal pins are assigned to the perimeter for ease of routing on the board. The package is offered in a die-up format and contains a wire-bond device covered with a mold compound. As shown in the cross section of Figure 5-1, the BGA package contains a wire- bond die on a single-core printed circuit board with an overmold.

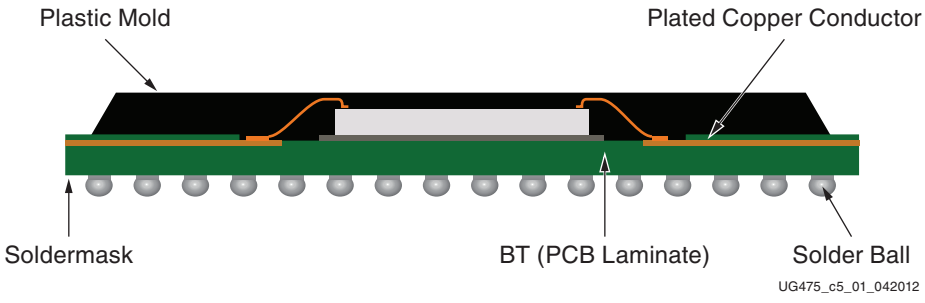

Figure 5-1: **Cavity-Up Ball Grid Array Package**

The key features/advantages of cavity-up BGA packages are:

- Low profile and small footprint
- Enhanced thermal performance
- Excellent board-level reliability

Wire-Bond Packages

Wire-bond packages meet the demands required by miniaturization while offering improved performance. Applications for wire-bond packages are targeted to portable and consumer products where board space is of utmost importance, miniaturization is a key requirement, and power consumption/dissipation must be low. By employing 7 series FPGA wire-bond packages, system designers can dramatically reduce board area requirements. Xilinx wire-bond packages are rigid BT-based substrates (see Figure 5-2).

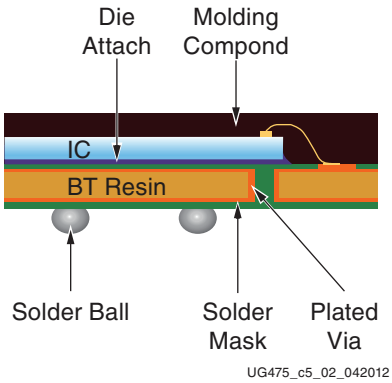

Figure 5-2: **Rigid BT-Based Substrate Wire-Bond Packages**

The key features/advantages of wire-bond packages are:

- An extremely small form factor which significantly reduces board area requirements for portable and wireless designs and PC add-in card applications.
- Lower inductance and lower capacitance
- The absence of thin, fragile leads found on other small package types
- A very thin, light-weight package

Flip-Chip Packages

For larger 7 series devices, Xilinx offers the flip-chip BGA packages, which present a low thermal path. These packages incorporate a heat spreader with additional thermal interface material (TIM), as shown in Figure 5-3.

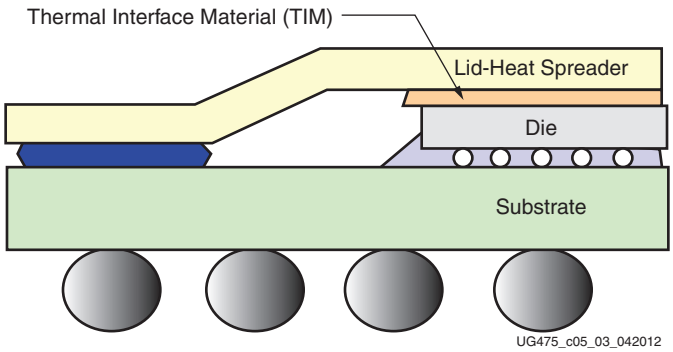

Figure 5-3: **Heat Spreader with Thermal Interface Material**

Materials with better thermal conductivity and consistent process applications deliver low thermal resistance up to the heat spreader. The junction-to-case thermal resistance (top of heat spreader) of all 7 series FPGA packages is typically less than 0.20°C/W. These packages deliver a low resistance platform for heat-sink applications.

A parallel effort to ensure optimized package electrical return paths produces the added benefit of enhanced power and ground plane arrangement in the packages. A boost in copper density on the planes improves the overall thermal conductivity through the laminate. In addition, the extra dense and distributed via fields in the package increase the vertical thermal conductivity. These packages offer up to 20% lower θ_{JB} compared to previous flip-chip packages.

Heat Sink Solutions at the System Level

Depending on the system's physical as well as mechanical constraints, the expectation is that an overall thermal budget is maintained with custom or OEM heat sink solutions, thus providing the third prong in the thermal management strategy. A heat-sink solution is managed by the system-level designer to tailors the design and solution to the specific system constraints with knowledge of the device's inherent capabilities for delivering heat to the surface. Heat-sink solutions are available and can be effective on these low θ_{JB} flip-chip platforms.

The packages used by 7 series devices can be described as medium or high-performance packages based on their power handling capabilities. All 7 series FPGA packages can benefit by using thermal enhancements, ranging from simple airflow calculations to schemes that include passive as well as active heat sinks. This is particularly true for the larger flip-chip BGA packages where system designers have the option to further enhance the packages with larger, more elaborate heat sinks to handle excesses of 25W with arrangements that consider both system and physical constraints.

Some Thermal Management Options

The flip-chip thermal management chart in Figure 5-4 illustrates incremental power management schemes that can be applied on a flip-chip BGA package.

Low End 1–6W	Bare package with moderate air 8–12°C/W	Bare package Package can be used with moderate airflow within a system
Mid Range 4–10W	Passive heat sink plus air 5–10°C/W	Package used with various forms of passive heat sinks Heat spreader techniques
High End 8–25W	Active heat sink 2–3°C/W or Better	Package used with active heat sinks TEC and board level heat spreader techniques

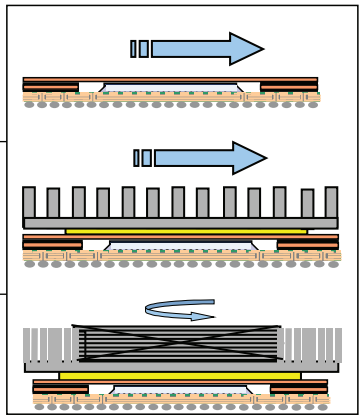

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Figure 5-4: **Thermal Management Options for Flip-Chip BGA Packages**

- For moderate power dissipation (less than 6W), the use of passive heat sinks and heat spreaders attached with thermally conductive double-sided tapes or retainers (with TIM around 0.2°C/W) offer quick thermal solutions in flip-chip BGA packages.
- The use of lightweight, finned, external, and passive heat sinks can be effective for dissipating up to 10-25W in the larger packages. Since the more efficient external heat sinks tend to be tall and heavy, additional design considerations can help protect component joints from heat sink induced stress cracks. Whenever a bulky heat sink is considered it is advisable to use spring-loaded pins or clips that transfer the mounting stress to a circuit board.
- The flip-chip BGA packages offered for 7 series devices are thermally enhanced BGAs with the die facing down (see Note). These packages have an exposed metal heat sink at the top. These high-end thermal packages lend themselves to the application of efficient external heat sinks (passive or active) for further heat removal efficiency. Precautions must be taken to prevent component damage when a bulky heat sink is attached. The thermal interface resistance needs to be controlled to take full advantage of these packages.

Note: Lidless (FB) packages are not thermally enhanced. See guidelines for applying heat sinks to lidless packages in Appendix B, Heat Sink Guidelines for Lidless Flip-Chip Packages.

- An active heat sink can include a simple heat sink incorporating a mini fan or even a Peltier Thermoelectric Cooler (TEC) with a fan to carry away any dissipated heat. When considering the use of a TEC for heat management, it is important to consult with experts about using the device because these devices can be reversed and cause damage to components. Also condensation can be an issue with these devices.
- The printed circuit board with a mounted device can have a significant impact on thermal performance. As much as 60 to 80% of the heat dissipated can go through the BGA balls directly to the board. A typical systems board is larger than the standard 4 x 4 inch JEDEC thermal board. Components mounted on these boards, with multiple copper layers and several internal vias, show low effective junction-to-ambient thermal resistances.

Table 5-2 shows this impact as an FF1156 flip-chip package's effective junction to ambient resistance is changed depending on the mounting board.

Table 5-2: **Impact of Mounted Board Characteristics on θ_{JA}(FF1156)**

		θ_{JA} (°C/W) for Different Board Sizes		
		4 x 4 in	10 x 10 in	20 x 20 in
Layer Count of Mounted Board	4	9.1 (1)	8.3	–
	8	8.0	5.5	4.9
	12	7.5	4.7	4.4
	16	7.2	4.5	4.2
	24	–	4.3	4.0

Notes:

1. Base JEDEC Mount Conditions

- Designs can be implemented to take advantage of the board's ability to spread heat. The effect of the board depends on its size and how it conducts heat. Board size, the level of copper traces, and the number of buried copper planes all lower the junction-to-ambient thermal resistance for a package mounted on the board. The cold ring junction-to-board thermal data for 7 series FPGA packages is listed in Table 5-1. Users must be aware that a direct heat path to the board from a component also exposes the component to the effect of other heat sources on the board, particularly if the board is not cooled effectively. An otherwise ambient component can be heated by other heat contributing components on the board.

Support for Compact Thermal Models (CTM)

Table 5-1 provides the traditional thermal resistance data for 7 series devices. These resistances are measured using a prescribed JEDEC standard that might not necessarily reflect the user's actual board conditions and environment. The quoted θ_{JA} and θ_{JC} numbers are environmentally dependent, and JEDEC has traditionally recommended that these be used with that awareness. For more accurate junction temperature prediction, these might not be enough, and a system-level thermal simulation might be required. Though Xilinx continues to support these figure of merit data, for 7 series FPGAs, boundary conditions independent compact thermal models (BCI-CTM) are also available to assist users in their thermal simulations.

Two-resistor as well as eight to ten-resistor network models are offered for all 7 series devices. These compact models seek to capture the thermal behavior of the packages more accurately at predetermined critical points (junction, case, top, leads, and so on) with the reduced set of nodes as illustrated in Figure 5-5.

Unlike a full 3D model, these are computationally efficient and work well in an integrated system simulation environment. Delphi CTM models are available on the Xilinx support download center (under the Device Model tab) at:

http://www.xilinx.com/support/download/index.htm

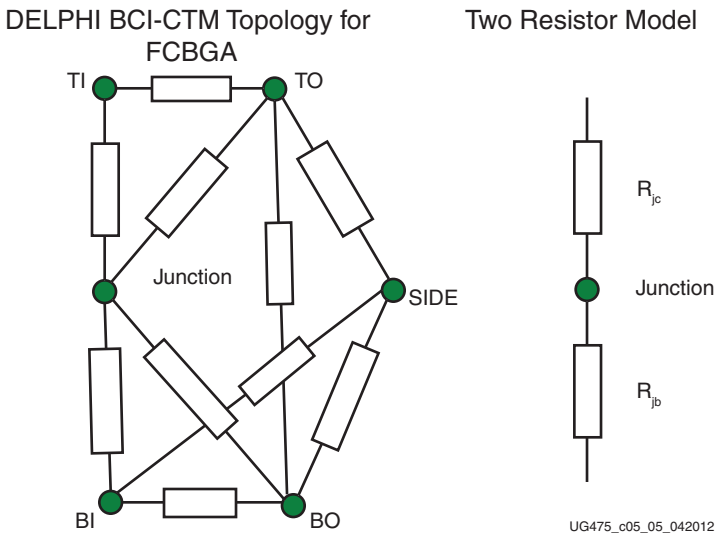

Figure 5-5: **Thermal Model Topologies**

The CTM models are based on the DELPHI approach that JEDEC has proposed. Since the JEDEC neutral (XML) format proposal has not been adopted yet, the DELPHI approach is used to generate these files and the data saved in the NATIVE and proprietary file formats of the targeted CFD tools - rather than follow a neutral file format. The CTM libraries are available in Flotherm (PDML) format – good for V5.1 and above and Icepack (version 4.2 and above) format.

Soldering Guidelines

To implement and control the production of surface-mount assemblies, the dynamics of the solder reflow process and how each element of the process is related to the end result must be thoroughly understood.

Note: Xilinx recommends that customers qualify their custom PCB assembly processes using package samples. UG112: *Device Package User Guide* contains further details on recommended assembly procedures.

The primary phases of the reflow process are:

1. Melting the particles in the solder paste
2. Wetting the surfaces to be joined
3. Solidifying the solder into a strong metallurgical bond

In a Pb-free soldering system, the sequences are the same. However, for the Pb-free soldering system, higher reflow temperature is applied. The peak reflow temperature of a plastic surface-mount component (PSMC) body should not be more than 220°C for standard packages and 245–260°C for Pb-free packages (package size dependent). For multiple BGAs in a single board and because of surrounding component differences, Xilinx recommends checking all BGA sites for varying temperatures.

The infrared reflow (IR) process is strongly dependent on equipment and loading. Components might overheat due to lack of thermal constraints. Unbalanced loading can lead to significant temperature variation on the board. These guidelines are intended to assist users in avoiding damage to the components; the actual profile should be determined by those using these guidelines. For complete information on package moisture / reflow classification and package reflow conditions, refer to the Joint IPC/JEDEC Standard J-STD-020C.

Sn/Pb Reflow Soldering

Figure 5-6 shows typical conditions for solder reflow processing of Sn/Pb soldering using IR/convection. Both IR and convection furnaces are used for BGA assembly. The moisture sensitivity of PSMCs must be verified prior to surface-mount flow.

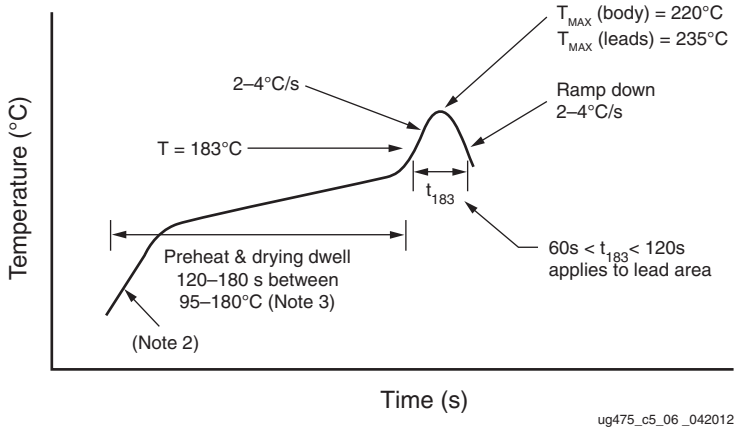

Figure 5-6: **Typical Conditions for IR Reflow Soldering of Sn/Pb Solder**

Notes for Figure 5-6:

1. Maximum temperature range = 220°C (body). Minimum temperature range before 205°C (leads/balls).
2. Preheat drying transition rate 2–4°C/s
3. Preheat dwell 95–180°C for 120–180 seconds
4. IR reflow must be performed on dry packages

Pb-Free Reflow Soldering

Xilinx uses SnAgCu solder balls for BGA packages. In addition, suitable material are qualified for the higher reflow temperatures (245°C–260°C) required by Pb-free soldering processes.

Xilinx does not recommend soldering BGA packages with SnPb solder using a Sn/Pb soldering process. Traditional Sn/Pb soldering processes have a peak reflow temperature of 220°C. At this temperature range, the SnAgCu BGA solder balls do not properly melt and wet to the soldering surfaces. As a result, reliability and assembly yields can be compromised.

The optimal profile must take into account the solder paste/flux used, the size of the board, the density of the components on the board, and the mix between large components and smaller, lighter components. Profiles should be established for all new board designs using thermocouples at multiple locations on the component. In addition, if there is a mixture of devices on the board, then the profile should be checked at various locations on the board. Ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that might damage the smaller, heat sensitive components.

Table 5-3 and Figure 5-7 provide guidelines for profiling Pb-free solder reflow.

In general, a gradual, linear ramp into a spike has been shown by various sources to be the optimal reflow profile for Pb-free solders (Figure 5-7). This profile has been shown to yield better wetting and less thermal shock than conventional ramp-soak-spike profile for the Sn/Pb system. SnAgCu alloy reaches full liquidus temperature at 235°C. When profiling, identify the possible locations of the coldest solder joints and ensure that those solder joints reach a minimum peak temperature of 235°C for at least 10 seconds. It might not be necessary to ramp to peak temperatures of 260°C and above. Reflowing at high peak temperatures of 260°C and above can damage the heat sensitive components and cause the board to warp. Users should reference the latest IPC/JEDEC J-STD-020 standard for the allowable peak temperature on the component body. The allowable peak temperature on the component body is dependent on the size of the component. Refer to Table 5-3 for peak package reflow body temperature information. In any case, use a reflow profile with the lowest peak temperature possible.

Table 5-3: **Pb-Free Reflow Soldering Guidelines**

Profile Feature	Convection, IR/Convection
Ramp-up rate	3°C/s maximum
Preheat Temperature 150°–200°C	60–120 seconds
Temperature maintained above 217°C	60–150 seconds (60–90 seconds typical)
Time within 5°C of actual peak temperature	30 seconds maximum

Table 5-3: **Pb-Free Reflow Soldering Guidelines *(Cont'd)***

Profile Feature	Convection, IR/Convection
Peak Temperature (lead/ball)	235°C minimum, 245°C typical (depends on solder paste, board size, components mixture)
Peak Temperature (body)	245°C–260°C, package body size dependent (reference Table 5-4)
Ramp-down Rate	6°C/s maximum
Time 25°C to Peak Temperature	3.5 minutes minimum, 5.0 minutes typical, 8 minutes maximum

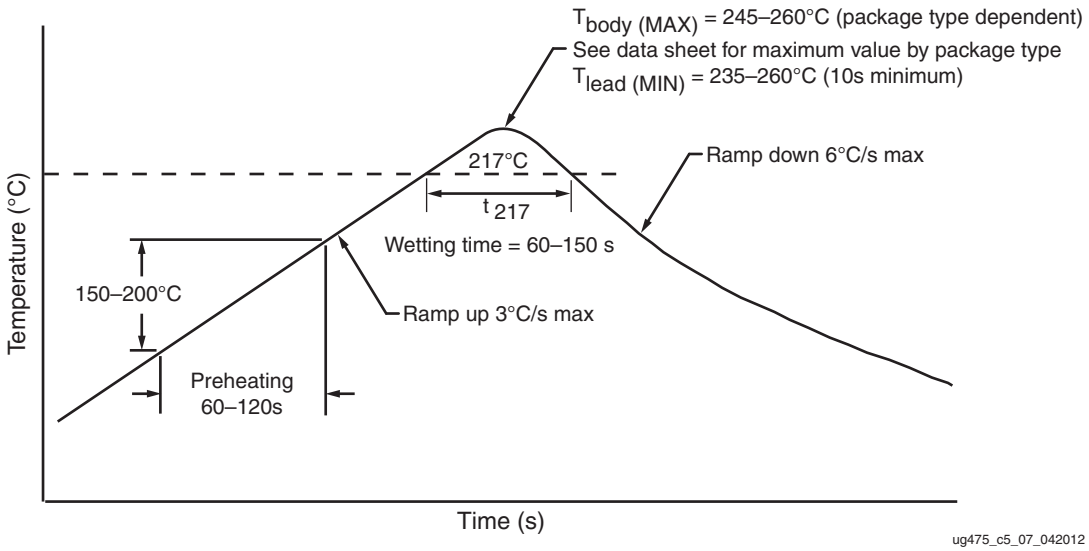

Figure 5-7: **Typical Conditions for Pb-Free Reflow Soldering**

Table 5-4: **Peak Package Reflow Body Temperature for Xilinx Pb-Free Packages (Based on J-STD-020 Standard)**

Package		Peak Package Reflow Body Temperature	JEDEC Moisture Sensitivity Level (MSL)
BGA			
Flip-Chip	FLG1925 FLG1926 FLG1928 FLG1930 FHG1761	Note 1	4
	HCG1155 HCG1931 HCG1932	Note 1	4
	SBG484 FBG484 FBG676 FBG900 FFG676 FFG900 FFG901 FFG1156 FFG1157 FFG1158 FFG1761 FFG1926 FFG1927 FFG1928 FFG1930	Note 1	4
Wire Bond	CSG324 FTG256 FGG484 FGG676	Note 1	3

Notes:

1. See specific 7 series device data sheets at: http://www.xilinx.com/support/documentation/7_series.htm#156339

For sophisticated boards with a substantial mix of large and small components, it is critical to minimize the ΔT across the board (<10°C) to minimize board warpage and thus, attain higher assembly yields. Minimizing the ΔT is accomplished by using a slower rate in the warm-up and preheating stages. Xilinx recommends a heating rate of less than 1°C/s during the preheating and soaking stages, in combination with a heating rate of not more than 3°C/s throughout the rest of the profile.

It is also important to minimize the temperature gradient on the component, between top surface and bottom side, especially during the cooling down phase. The key is to optimize cooling while maintaining a minimal temperature differential between the top surface of

the package and the solder joint area. The temperature differential between the top surface of the component and the solder balls should be maintained at less than 7°C during the critical region of the cooling phase of the reflow process. This critical region is in the part of the cooling phase where the balls are not completely solidified to the board yet, usually between the 200°C–217°C range. To efficiently cool the parts, divide the cooling section into multiple zones, with each zone operating at different temperatures.

For more information on Xilinx Pb-free solutions, refer to:

http://www.xilinx.com/system_resources/lead_free/index.htm.

For more information on the Pb-free reflow process, refer to XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

References

The following websites contain additional information on heat management and contact information.

- http://www.wakefield.com
- http://www.aavidthermalloy.com
- http://www.qats.com

Refer to the following websites for interface material sources:

- Power Devices - http://www.powerdevices.com
- Bergquist Company - http://www.bergquistcompany.com
- AOS Thermal Compound - http://www.aosco.com
- Chometrics - http://www.chomerics.com
- Kester - http://www.kester.com

Refer to the following websites for CFD tools Xilinx supports with thermal models.

- Flomerics - Flotherm & FloPCB - http://www.flomerics.com
- Fluent - Icepak - http://www.icepak.com

Chapter 6

Package Marking

All 7 series devices have package top-markings similar to the examples shown in Figure 6-1, Figure 6-2, and Figure 6-3. The markings are explained in Table 6-1.

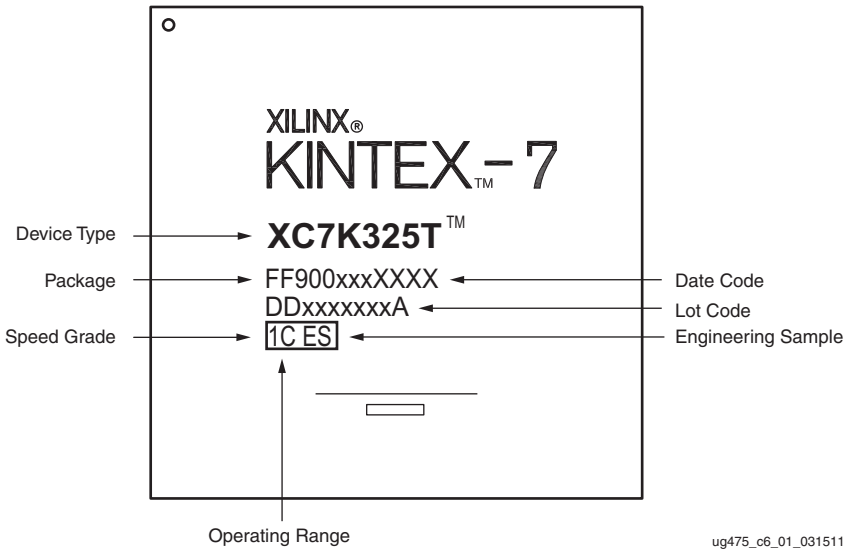

Figure 6-1: **Kintex-7 Device Package Marking**

Figure 6-2: **Virtex-7 Device Package Marking**

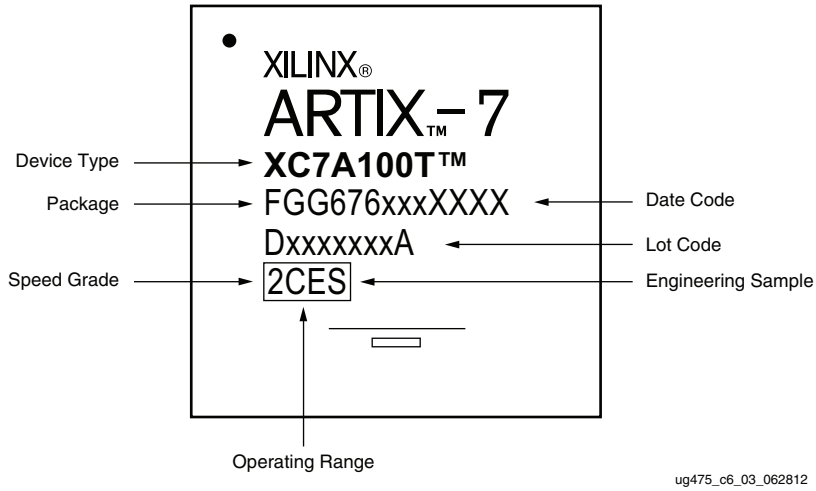

Figure 6-3: **Artix-7 Device Package Marking**

Table 6-1: **Xilinx Device Marking Definition—Example**

Item	Definition
Xilinx Logo	Xilinx logo, Xilinx name with trademark, and trademark-registered status.
Family Brand Logo	Device family name with trademark and trademark-registered status. This line is optional and could appear blank.
1st Line	Device type.
2nd Line	Package code, circuit design revision, the location code for the wafer fab, the geometry code, and date code. A *G* in the third letter of a package code indicates a Pb-free RoHS compliant package. For more details on Xilinx Pb-Free and RoHS Compliant Products, see: http://www.xilinx.com/pbfree.

Table 6-1: **Xilinx Device Marking Definition—Example *(Cont'd)***

Item	Definition	
3rd Line	Ten alphanumeric characters for Assembly, Lot, and Step information. The last digit is usually an *A* or an *M* if a stepping version does not exist.	
4th Line	Device speed grade and temperature range. When not marked on the package, the product is considered to operate at the commercial (C) temperature range. For more information on the ordering codes, see DS180: *7 Series FPGAs Overview*. Other variations for the 4th line:	
	L2E	The *L2E* indicates a -2LE device. The -2L devices operate at either of two voltages, 0.9V and 1.0V. The E is for the extended temperature operating range. For more information, see the specific device's data sheet at: http://www.xilinx.com/support/documentation/7_series.htm#156339.
	1C xxxx	The *xxxx* indicates the SCD for the device. An SCD is a special ordering code that is not always marked in the device top mark.
	1C ES	The *ES* indicates an Engineering Sample.

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Appendix A

Recommended PCB Design Rules for BGA Packages

Xilinx provides the diameter of a land pad on the component side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are described in Figure A-1 and summarized in Table A-1. For Xilinx® BGA packages, Non-Solder Mask Defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure A-1. The space between the NSMD pad and the solder mask as well as the actual signal trace widths depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

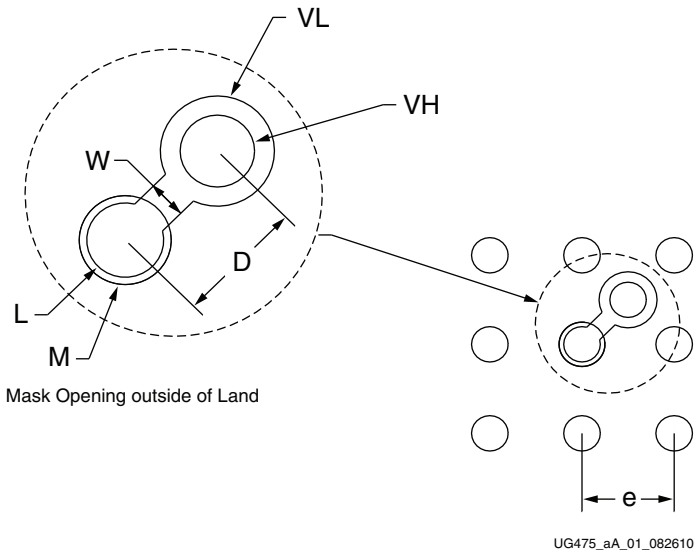

Figure A-1: **Suggested Board Layout of Soldered Pads for BGA Packages**

Table A-1: **Recommended PCB Design Rules for All FFG/FHG/FLG/HCG Packages**

Design Rule	FFG/FHG/FLG/HCG Packages (Dimensions in mm)
Component Land Pad Diameter (SMD)(1)	0.53
Solder Land (L) Diameter	0.45
Opening in Solder Mask (M) Diameter	0.55
Solder (Ball) Land Pitch (e)	1.00
Line Width Between Via and Land (w)	0.13
Distance Between Via and Land (D)	0.70
Via Land (VL) Diameter	0.61
Through Hole (VH) Diameter	0.300

Notes:

1. Component land pad diameter refers to the pad opening on the component side (solder mask defined).

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Appendix B

Heat Sink Guidelines for Lidless Flip-Chip Packages

Heat Sink Attachments for Lidless FCBGA (FB/FBG)

Heat sinks can be attached to the package in multiple ways. For heat to dissipate effectively, the advantages and disadvantages of each heat sink attachment method must be considered. Factors influencing the selection of the heat sink attachment method include the package type, contact area of the heat source, and the heat sink type.

Silicon and Decoupling Capacitors Height Consideration

When designing heat sink attachments for lidless flip-chip BGA (FCBGA) packages, the height of the die above the substrate and also the height of decoupling capacitors must be considered (Figure B-1). This is to prevent electrical shorting between the heat sink (metal) and the decoupling capacitors.

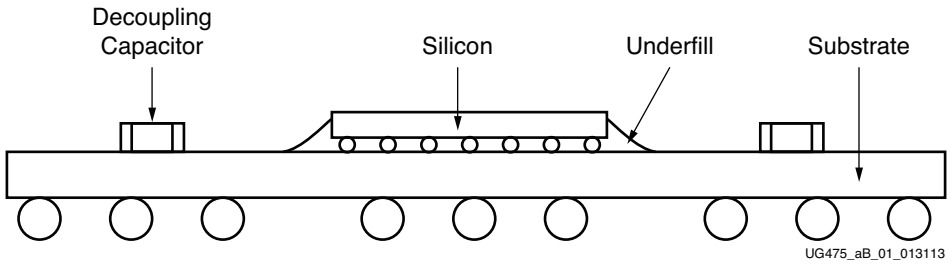

Figure B-1: **Cross Section of Lidless Flip-chip BGA**

Types of Heat Sink Attachments

There are six main methods for heat sink attachment. Table B-1 lists their advantages and disadvantages.

- Thermal tape
- Thermally conductive adhesive or glue (epoxy)
- Wire form Z-clips
- Plastic clip-ons
- Threaded stand-offs (PEMs) and compression springs
- Push-pins and compression springs

Table B-1: **Heat Sink Attachment Methods**

Attachment Method	Advantages	Disadvantages
Thermal tape	• Generally easy to attach and is inexpensive. • Lowest cost approach for aluminum heat sink attachment. • No additional space required on the PCB.	• The surfaces of the heat sink and the chip must be very clean to allow the tape to bond correctly. • Because of the small contact area, the tape might not provide sufficient bond strength. • Tape is a moderate to low thermal conductor that could affect the thermal performance.
Thermally conductive adhesive or glue	• Outstanding mechanical adhesion. • Fairly inexpensive, costs a little more than tape. • No additional space required on the PCB.	• Adhesive application process is challenging and it is difficult to control the amount of adhesive to use. • Difficult to rework. • Because of the small contact area, the adhesive might not provide sufficient bond strength.
Wire form Z-clips	• It provides a strong and secure mechanical attachment. In environments that require shock and vibration testing, this type of strong mechanical attachment is necessary. • Easy to apply and remove. Does not cause the semiconductors to be destroyed (epoxy and occasionally tape can destroy the device). • It applies a preload onto the thermal interface material (TIM). Pre-loads actually improve thermal performance.	• Requires additional space on the PCB for anchor locations.
Plastic clip-ons	• Suitable for designs where space on the PCB is limited. • Easy to rework by allowing heat sinks to be easily removed and reapplied without damaging the PCB board. • Can provide a strong enough mechanical attachment to pass shock and vibration test.	• Needs a keep out area around the silicon devices to use the clip. • Caution is required when installing or removing clip-ons because localized stress can damage the solder balls or chip substrate.
Threaded stand-offs (PEMs) and compression springs	• Provides stable attachments to heat source and transfers load to the PCB, backing plate, or chassis. • Suitable for high mass heat sinks. • Allows for tight control over mounting force and load placed on chip and solder balls.	• Holes are required in the PCB taking valuable space that can be used for trace lines. • Tends to be expensive, especially since holes need to be drilled or predrilled onto the PCB board to use stand-offs.
Push-pins and compression springs	• Provides a stable attachment to a heat source and transfers load to the PCB. • Allows for tight control over mounting force and load placed on chip and solder balls.	• Requires additional space on the PCB for push-pin locations.

Heat Sink Attachment

Component Pick-up Tool Consideration

For pick-and-place machines to place lidless FCBGAs onto PCBs, Xilinx recommends using soft tips or suction cups for the nozzles. This prevents chipping, scratching, or even cracking of the bare die (Figure B-2).

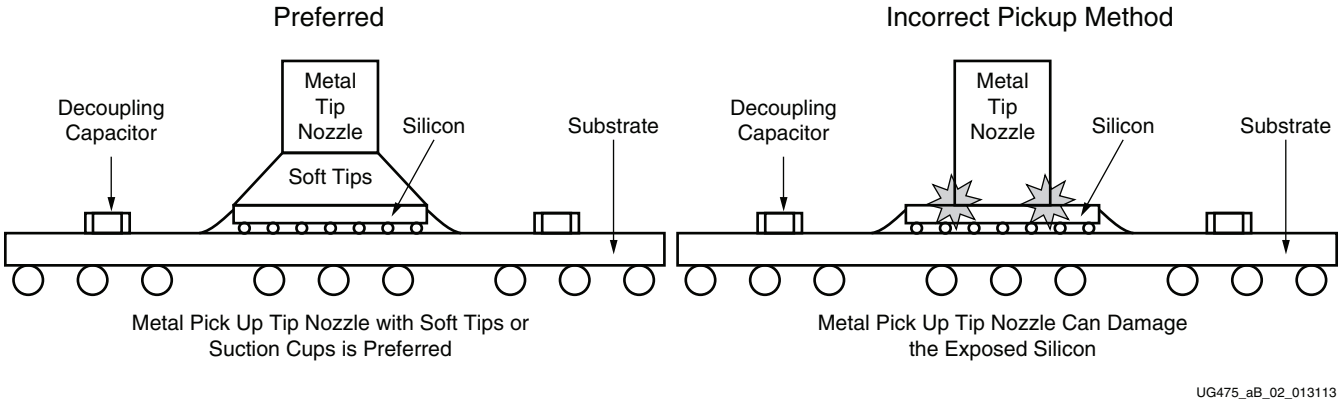

Figure B-2: **Recommended Method For Using Pick-up Tools**

Heat Sink Attachment Process Considerations

After the component is placed onto the PCBs, when attaching a heat sink to the lidless package, the factors in Table B-2 must be carefully considered (see Figure B-3).

Table B-2: **Heat Sink Attachment Considerations**

Consideration(s)	Effect(s)	Recommendation(s)
In heat sink attach process, what factors can cause damage to the expose die and passive capacitors?	• Uneven heat sink placement • Uneven TIM thickness • Uneven force applied when placing heat sink placement	• Even heat sink placement • Even TIM thickness • Even force applied when placing heat sink placement
Does the heat sink tilt or tip the post attachment?	Uneven heat sink placement will damage the silicon and can cause field failures.	• Careful handling not to contact the heat sink with the post attachment. • Use a fixture to hold the heat sink in place with post attachment until it is glued to the silicon.

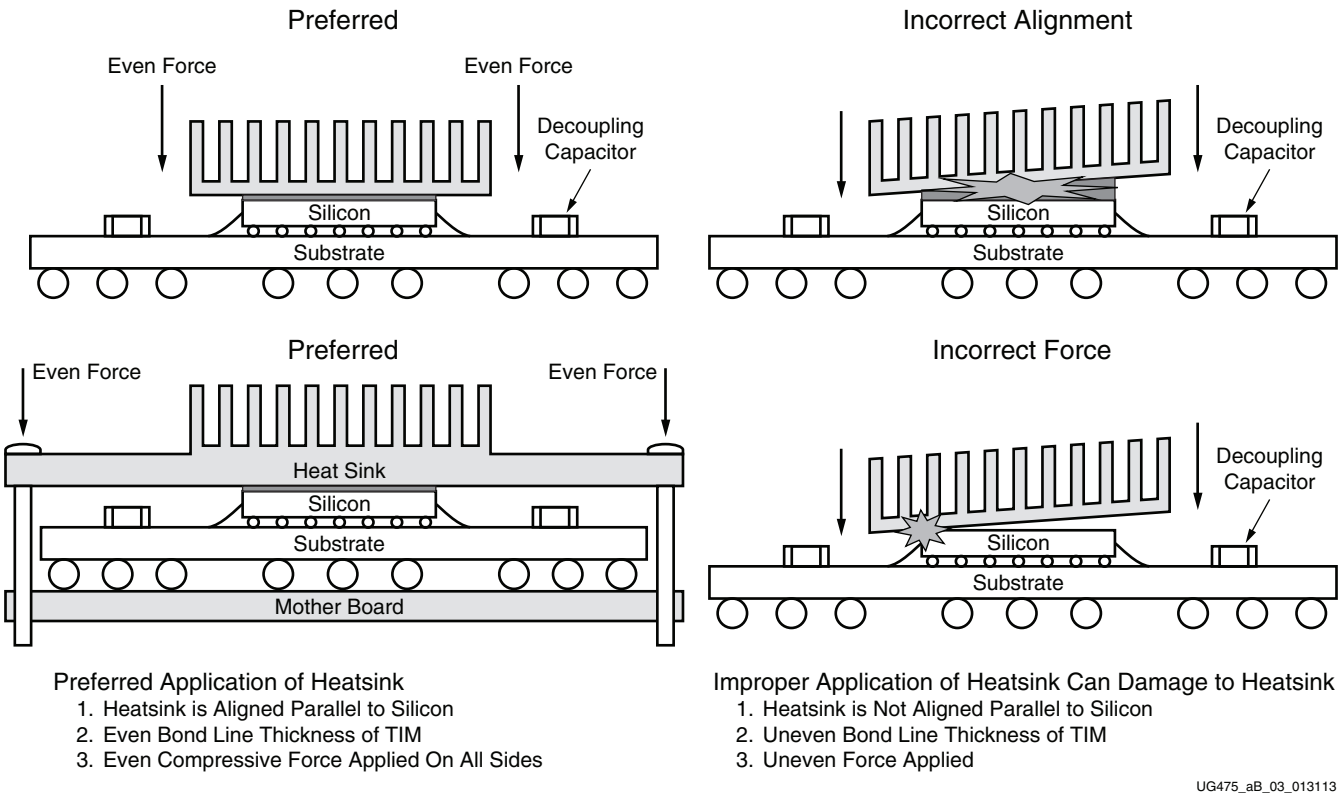

Figure B-3: **Recommended Application of Heat Sink**

Standard Heat Sink Attach Process with Thermal Conductive Adhesive

Prior to attaching the heat sink, the FPGA needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermoset material (electrically non-conductive) is applied over the backside surface of silicon in a pattern using automated dispensing equipment. Automated dispensers are often used to provide a stable process speed at a relatively low cost. The optimum dispensing pattern needs to be determined by the SMT supplier.

   Note: Minimal volume coverage of the backside of the silicon can result in non-optimum heat transfer.
3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the adhesive spreads to cover the backside silicon. A force transducer is normally used to measure and limit the placement force.
4. The epoxy is cured with heat at a defined time.

   Note: The epoxy curing temperature and time is based on manufacturer's specifications.

Standard Heat Sink Attach Process with Thermal Adhesive Tape

Prior to attaching the heat sink, the FPGA needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermal adhesive tape cut to the size of the heat sink is applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.
3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the thermal adhesive tape is glued to the backside of the silicon. A force transducer is normally used to measure and limit the placement force.
4. A uniform and constant pressure is applied uniformly over the heat sink and held for a defined time.

   Note: The thermal adhesive tape hold time is based on manufacturer's specifications.

Push-Pin and Shoulder Screw Heat Sink Attachment Process with Phase Change Material (PCM) Application

Prior to attaching the heat sink, the FPGA needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.

   Note: The jig or fixture needs to account for the push pin depth of the heat sink.
2. PCM tape, cut to the size of the heat sink, os applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.
3. Using the push-pin tool, heat sinks are applied over the packages ensuring a pin locking action with the PCB holes. The compression load from springs applies the appropriate mounting pressure required for proper thermal interface material performance.

   Note: Heat sinks must not tilt during installation. This process cannot be automated due to the mechanical locking action which requires manual handling. The PCB drill hole tolerances need to be close enough to eliminate any issues concerning the heat sink attachment.

Package Loading Specifications

For lidless FCBGA, Xilinx specifies a maximum static load of 60 psi. This mechanical maximum load limit cannot be exceeded during heat sink assembly, shipping conditions, or standard use conditions. Any mechanical system or component testing must not exceed the maximum limit.

The static load of maximum 60 psi is:

- Applied as uniform compressive loading in a direction normal to the package.
- The maximum allowed load from the heat sink retention clip.
- Based on limited testing for design characterization. Loading limits are for the package only.

Note: As a precaution; a minimum point force of 75 ft-lbs can cause the die to crack.

For thermal and mechanical solutions, the package substrate must not be used as a mechanical reference or load-bearing surface. For heat sink clip pre-load calculations, the post-reflow package height must be used.

Reasons for Thermal Interface Material

When installing heat sinks for Xilinx FPGAs, a suitable thermal interface material (TIM) must be used. This thermal material significantly aids the transfer of heat from the component to the heat sink. For optimum heat transfer, Xilinx recommends the use of thermal interface materials.

For lidless FCBGAs, the surface of the silicon contacts the heat sink. For lidded FCBGAs, the lid contacts the heat sink. The surface size of the lidless FCBGA and lidded FCBGA are different. Xilinx recommends a different type of thermal material for long-term use with each type of FCBGA package.

Thermal interface material is needed because even the largest heat sink and fan cannot effectively cool an FPGA unless there is good physical contact between the base of the heat sink and the top of the FPGA. The surfaces of both the heat sink and the FPGA silicon are not absolutely smooth. This surface roughness is observed when examined at a microscopic level. Because surface roughness reduces the effective contact area, attaching a heat sink without a thermal interface material is not sufficient due to inadequate surface contact.

A thermal interface material such as phase-change material, thermal grease, or thermal pads fills these gaps and allows effective transference of heat between the FPGA die and the heat sink.

Types of TIM

There are many type of TIM available for sale. The most commonly used thermal interface materials are:

- Thermal pads, also called phase-change materials.
- Thermal grease, also called thermal paste.

Phase-change materials are usually thin pads approximately 1 inch x 1 inch (2.5 cm x 2.5 cm) in size and have protective films attached on both surfaces. The color is vendor-specific but is usually gray or pink. Thermal grease usually comes in a syringe, a tube, or a small plastic sachet. Thermal grease is similar in consistency to ordinary toothpaste and is typically gray or white.

Guidelines for Thermal Interface Materials

Five factors affect the choice, use, and performance of the interface material used between the processor and the heat sink:

- Thermal Conductivity of the Material
- Electrical Conductivity of the Material
- Spreading Characteristics of the Material
- Long-Term Stability and Reliability of the Materiall
- Ease of Application

Thermal Conductivity of the Material

Thermal conductivity is the quantified ability of any material to transfer heat. The thermal conductivity of the interface material has a significant impact on its thermal performance. The higher the thermal conductivity, the more efficient the material is at transferring heat. Materials that have a lower thermal conductivity are less efficient at transferring heat,

causing a higher temperature differential to exist across the interface. To overcome this less efficient heat transfer, a better cooling solution (typically, a more costly solution) must be used to achieve the desired heat dissipation.

Electrical Conductivity of the Material

Some metal-based TIM compounds are electrically conductive. Ceramic-based compounds are typically not electrically conductive. Manufacturers produce metal-based compounds with low-electrical conductivity, but some of these materials are not completely electrically inert. Metal-based thermal compounds are not hazardous to the FPGA die itself, but other elements on the FPGA or motherboard can be at risk if they become contaminated by the compound. For this reason, Xilinx does not recommend the use of electrically conductive thermal interface material.

Spreading Characteristics of the Material

The spreading characteristics of the thermal interface material determines its ability, under the pressure of the mounted heat sink, to spread and fill in or eliminate the air gaps between the FPGA and the heat sink. Because air is a very poor thermal conductor, the more completely the interface material fills the gaps, the greater the heat transference.

Long-Term Stability and Reliability of the Material

The long-term stability and reliability of the thermal interface material is described as the ability to provide a sufficient thermal conductance even after an extended time or extensive. Low-quality compounds can harden or leak out over time (the pump-out effect), leading to overheating or premature failure of the FPGA. High-quality compounds provide a stable and reliable thermal interface material throughout the lifetime of the device. Thermal greases with higher viscosities are typically more resistant to pump out effects on lidless devices.

Ease of Application

A spreadable thermal grease requires the surface mount supplier to carefully use the appropriate amount of material. Too much or too little material can cause problems. The thermal pad is a fixed size and is therefore easier to apply in a consistent manner.

Comparing the Types of Interface Materials

Thermal Grease

Thermal grease is a paste made up of thermally conductive ceramic fillers in silicone or hydrocarbon oils. It is applied to one of the two mating surfaces. When the surfaces are pressed together, the grease spreads to fill the void. See Table B-3 for the thermal resistance, and pros and cons of usage.

Table B-3: **Thermal Grease**

Thermal Resistance	Pros	Cons
0.2 to 1°C cm^2/W	• Eliminates air gaps between components and the heat sink. • Compensates for uneven heat sink surface and silicon. • It is soft and is easy to compress to the height differential of multiple components. • Stress-free with outstanding mechanical shock absorption.	• Hard to use in manufacturing because it is difficult to dispense and apply due to a high viscosity. • Requires cleanup to prevent contamination problems. • Requires mechanical clamping to hold the heat sink and component in its place. • Applications with repeated power on/off cycles might cause occurrence of pump-out, where the grease is forced from between the silicon die and the heat sink each time the die is heated up and cooled down. This can cause thermal performance degradation over time and contaminate the neighboring components.

Thermal Gel

Thermal gels are dispensed like thermal grease. They are cured to a partially cross-linked structure, which eliminates the pump-out issue. See Table B-4 for the thermal resistance, and pros and cons of usage.

Table B-4: **Thermal Gel**

Thermal Resistance	Pros	Cons
0.15 to 1°C cm^2/W	• No pump out issues. • Eliminates air gaps between components and the heat sink. • Compensates for uneven heat sink surface and silicon. • It is soft and is easy to compress to the height differential of multiple components. • Stress-free with outstanding mechanical shock absorption.	• A mechanical fastener is essential to maintain the joint once it is assembled.

Thermal Conductive Compound

A thermally conductive compound incorporates thermally conductive fillers. However, unlike thermal greases, the binder is a rubber material. When first applied, the paste-like compound flows into the interstices between the mating surfaces. Then, when subjected to heat, it cures into a dry rubber film. Besides its thermal properties, this film also serves as an adhesive, allowing a tight, void-free joint without the need for additional fasteners. Thermally conductive compounds can successfully fill larger gaps in situations where thermal greases might ooze from the joint. Although application and performance is similar to that of thermal grease, cleanup is easier, simply involving removal of the excess cured rubber film. See Table B-5 for the thermal resistance, and pros and cons of usage.

Table B-5: **Thermal Conductive Compound**

Thermal Resistance	Pros	Cons
0.15 to 1°C cm^2/W	• Mechanical clamping not required.	• Cannot be reworked. • Metal-based conductive adhesives can cause electrical shorting with contamination on the FPGAs and other devices on the motherboard.

Thermally Conductive Elastomeric Pads

Thermally conductive elastomeric pads consist of a silicone elastomer filled with thermally conductive ceramic particles and can incorporate woven glass fiber or dielectric film reinforcement. Typically, the recommended thickness is from 0.1 mm to 1 mm. The recommended hardness rating is from 5 to 85 Shore A. By providing both electrical insulation and thermal conductivity, they are useful in applications requiring electrical isolation. Thicker pads are used when large gaps must be filled. During application, the pads are compressed between the mating surfaces to make them conform to surface irregularities. See Table B-6 for the thermal resistance, and pros and cons of usage.

Table B-6: **Thermally Conductive Elastomeric Pads**

Thermal Resistance	Pros	Cons
1 to 3°C cm^2/W	• Simple assembly.	• A mechanical fastener is essential to maintain the joint once it is assembled. • Mounting pressure must be adjusted according to the hardness of the elastomer to ensure that voids are filled.

Thermal Tapes

A thermal tape is a double-sided pressure sensitive adhesive film filled with thermally conductive ceramic powder. To facilitate handling, aluminum foil or a polyimide film can be used to support the tape; the latter material also provides electrical insulation. When applied between mating surfaces, the tape must be subjected to pressure to conform to the surfaces. Once the joint is made, the adhesive holds it together permanently, eliminating the need for supplemental fasteners. No bond curing is needed. See Table B-7 for the thermal resistance, and pros and cons of usage.

Table B-7: **Thermal Tapes**

Thermal Resistance	Pros	Cons
1 to 4°C cm^2/W	• Simple assembly. • Mechanical clamping not required.	• Cannot fill large gaps between mating surfaces as well as liquids, which can affect thermal performance.

Phase Change Materials

Solid at room temperature, phase change materials are melted (i.e., undergo a phase change) as the temperature rises to the 104°F to 158°F (40°C to 70°C) range. This makes the material (0.13 mm thick in its dry film form) as easy to handle as a pad, while assuring that it will, when subjected to heat during the assembly process, flow into voids between

mating surfaces as effectively as a thermal grease. Ordinarily, applying power to the electronic component introduces the needed heat for the phase change to occur, establishing a stable thermal joint. These materials consist of organic binders (i.e., a polymer and a low-melt-point crystalline component, such as a wax), thermally conductive ceramic fillers, and, if necessary, a supporting substrate, such as aluminum foil or woven glass mesh. See Table B-7 for the thermal resistance, and pros and cons of usage.

Table B-8: **Phase Change Materials**

Thermal Resistance	Pros	Cons
0.3 to 0.7°C cm^2/W	• Simple assembly. • Mechanical clamping not required.	• Cannot be reworked. • A mechanical fastener is essential to maintain the joint once it is assembled.

Thermal Material Handling Guidelines

When not familiar with installing the heat sink on an FPGA, the assistance of a professional system builder, such as Sanmina (http://www.sanmina.com/) is warranted. Incorrect handling or assembling of FPGA components can damage parts, void the warranty, and lead to disappointing results.

If a chosen heat sink does not include the thermal interface material, inexperienced users should request recommendations from Xilinx.

Before applying any interface material, always make sure that the surfaces are clean and free of foreign materials. If the surface of the heat sink or FPGA becomes soiled or greasy, use a lint-free wipe or cloth and a mild solvent such as denatured alcohol to clean it.

Never reuse a thermal interface material. To reuse a heat sink, remove any residue of the previously used thermal material with a nonmetallic object like a plastic spatula and then use a lint-free wipe or cloth and a mild solvent such as denatured alcohol to fully cleanse the surface. Reapply a new thermal interface material.